

I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems

M. Murakami, H. Kobayashi, **S. N. B. Mohyar**
O. Kobayashi, T. Miki, J. Kojima

Gunma University

Universiti Malaysia Perlis

D-Clue Tech, formerly STARC



Research Objective

- To develop usage of complex multi-band signals for LSI testing applications
- To develop digital centric design of complex multi-band signal generator
 - Multi-bit $\Delta\Sigma$ DA modulator
 - Linearity enhancement algorithms

Outline

- Background to This Research
- Complex Multi-Band Signals
- Complex Multi-BP $\Delta\Sigma$ DA Modulators
- DWA Algorithm
- Self-Calibration
- Combination of DWA and Self-Calibration
- Conclusions

Outline

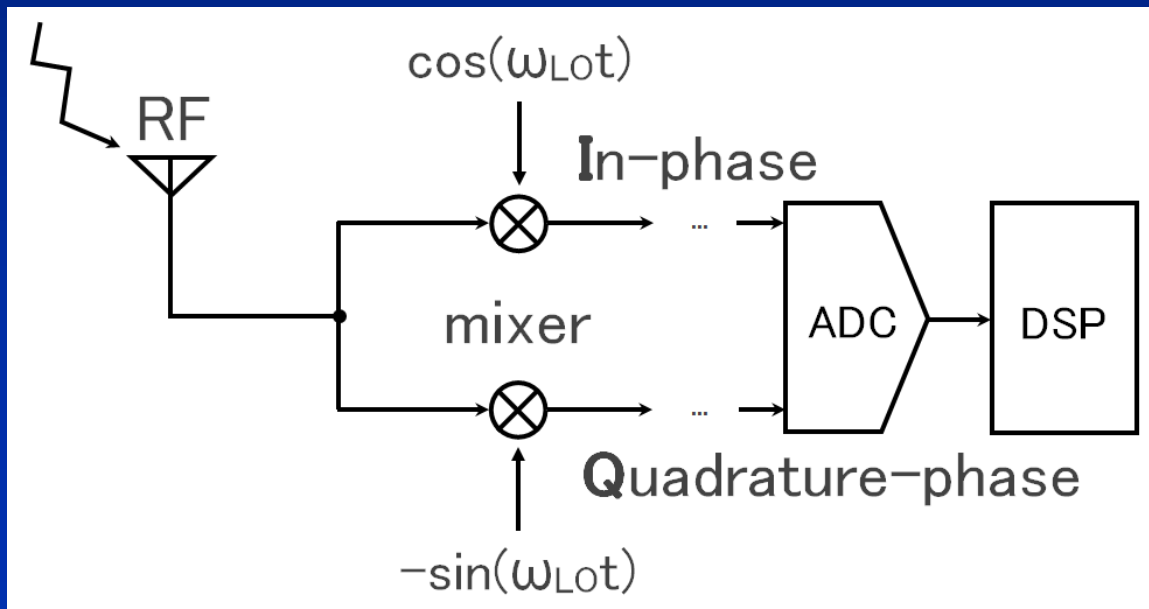
- Background to This Research
- Complex Multi-Band Signals
- Complex Multi-BP $\Delta\Sigma$ DA Modulators
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- Conclusions

Research Goal

Demand for low cost testing
of communication IC



High quality I,Q test signal generation for
receiver IC with low cost



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- Background to This Research
- **Complex Multi-Band Signals**
- Complex Multi-BP $\Delta\Sigma$ DA Modulators
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Complex Signal

2 Real signals

I_{in} , Q_{in}



Complex signal

$I_{in} + j Q_{in}$

$j = \sqrt{-1}$

Complex signal processing is NOT complex.

- Prof. Ken Martin, Toronto Univ.

Complex Signal in Frequency Domain

Complex signal

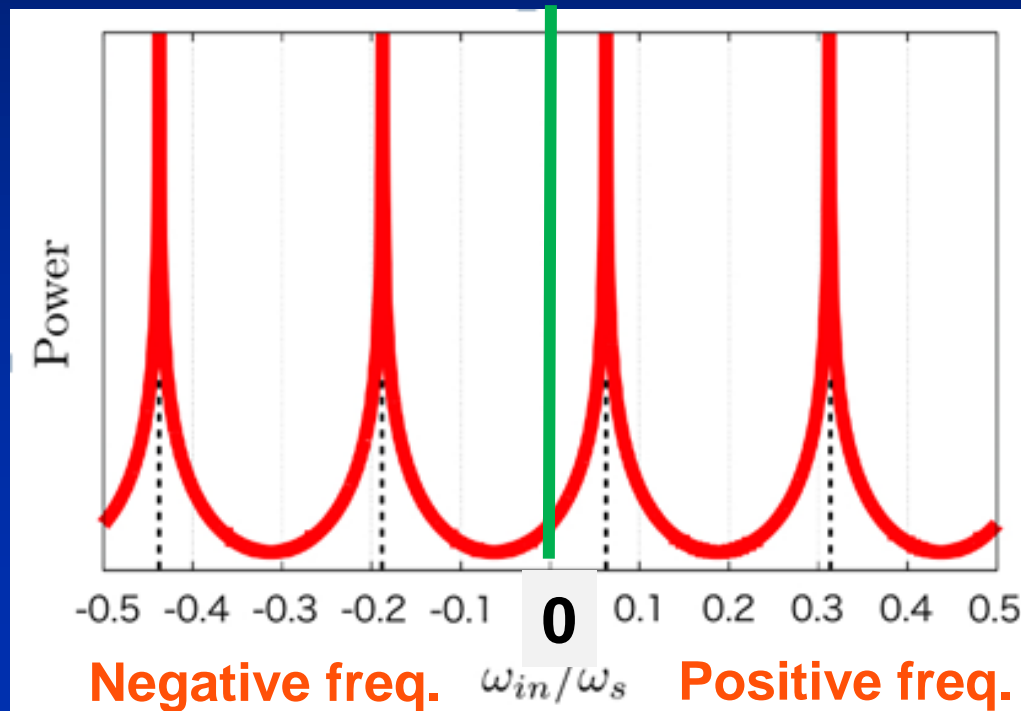
$$I_{in} + j Q_{in}$$

After Fourier transform

$$I_{in}(j\omega) + j Q_{in}(j\omega)$$

Asymmetric

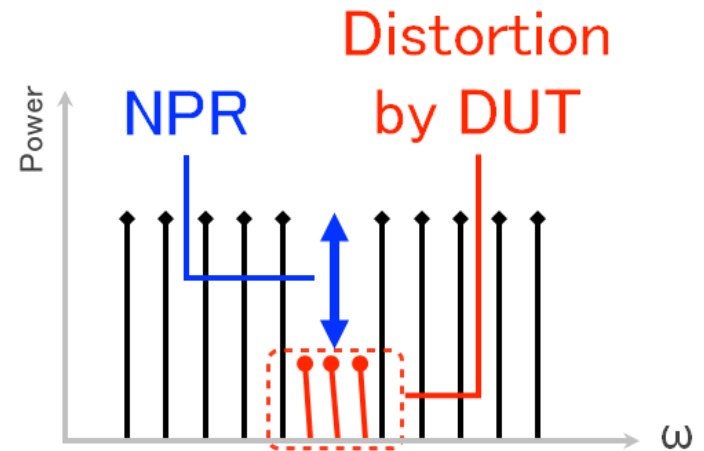
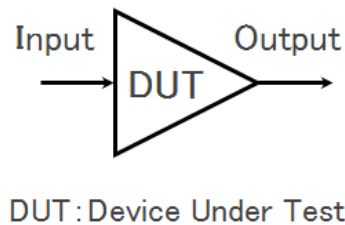
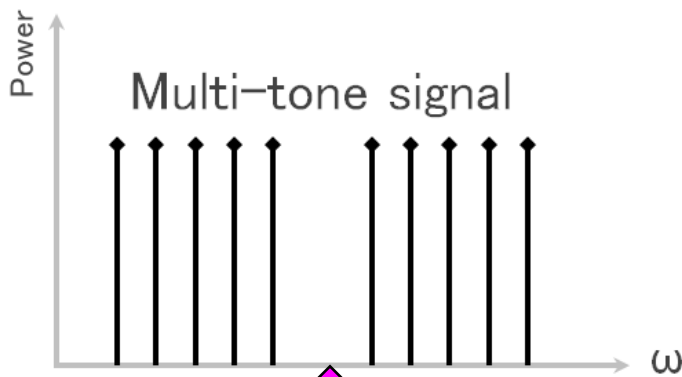
Complex



IC Testing with Multi-tone Signal

ADSL ADC Testing

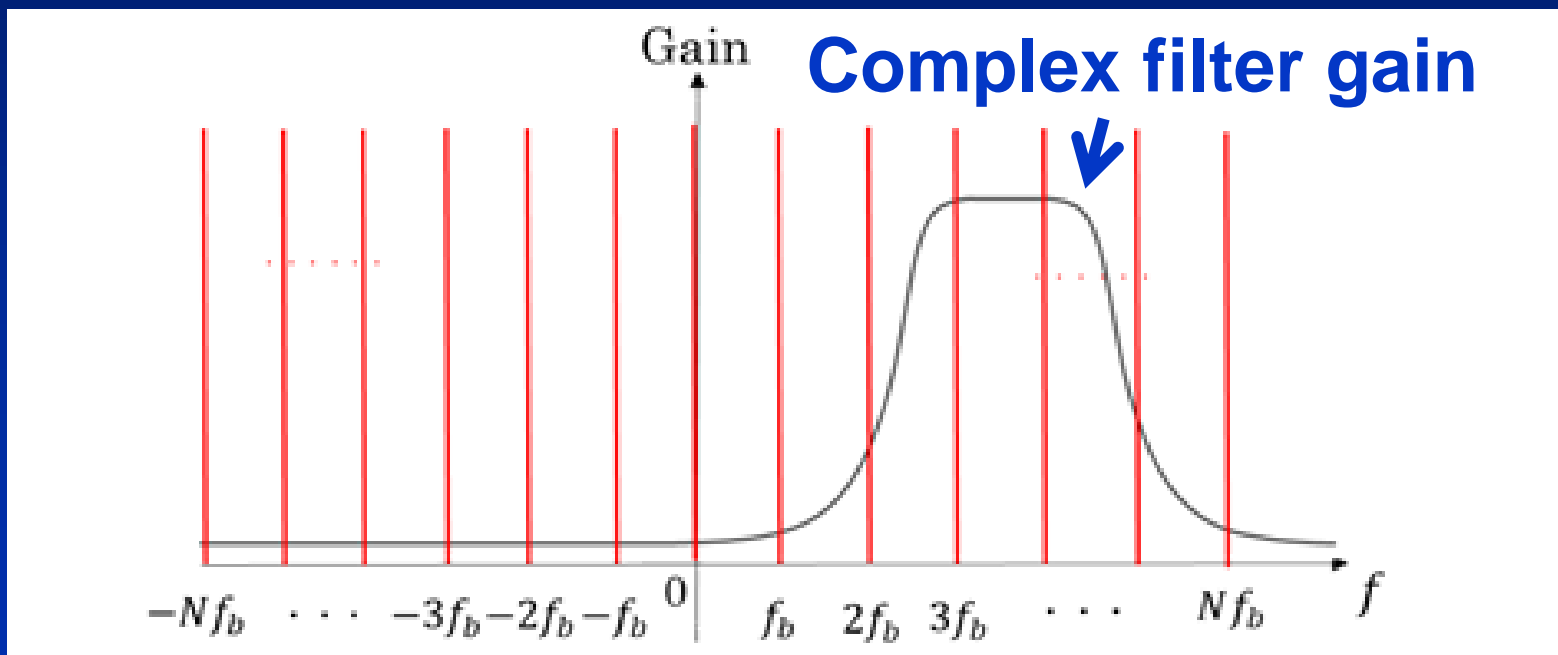
Noise Power Ratio (NPR)



empty

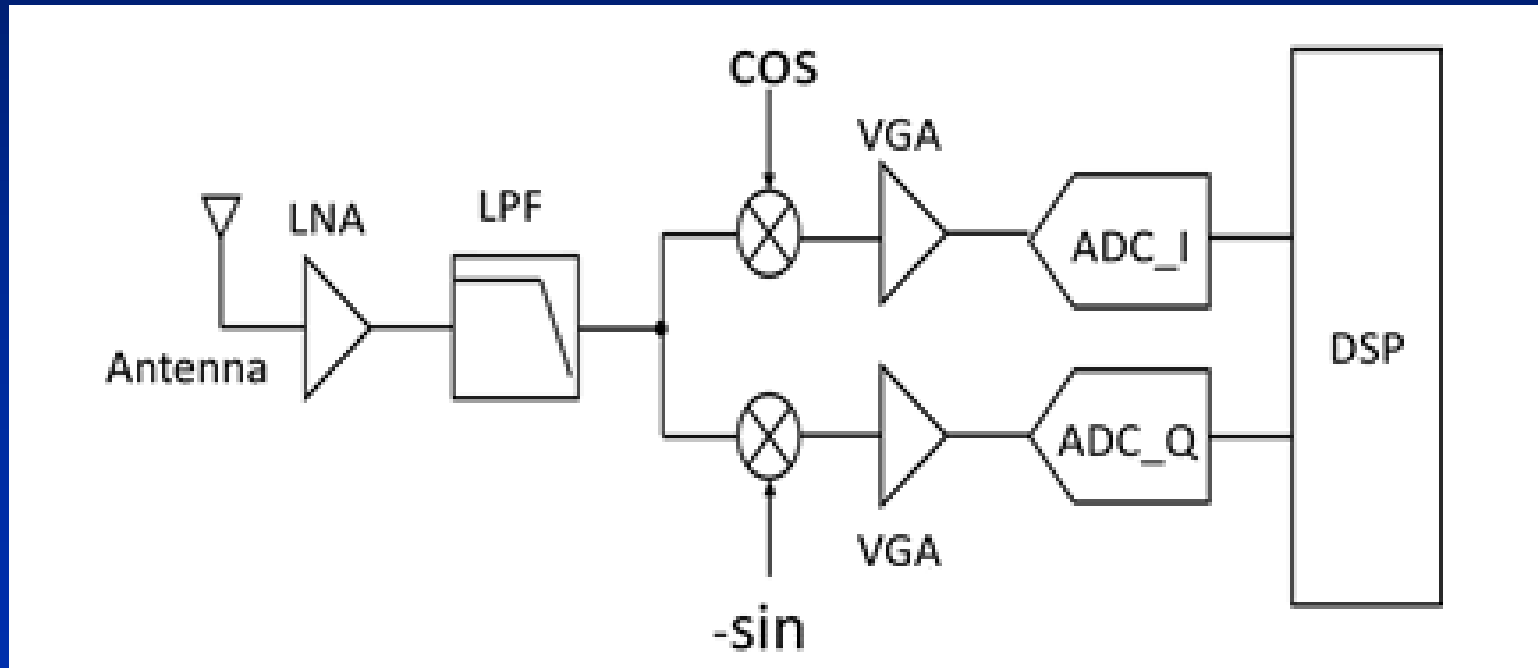
IC Testing with Complex Multi-tone Signal

Complex Analog Filter Testing



IC Testing with Complex Multi-tone Signal

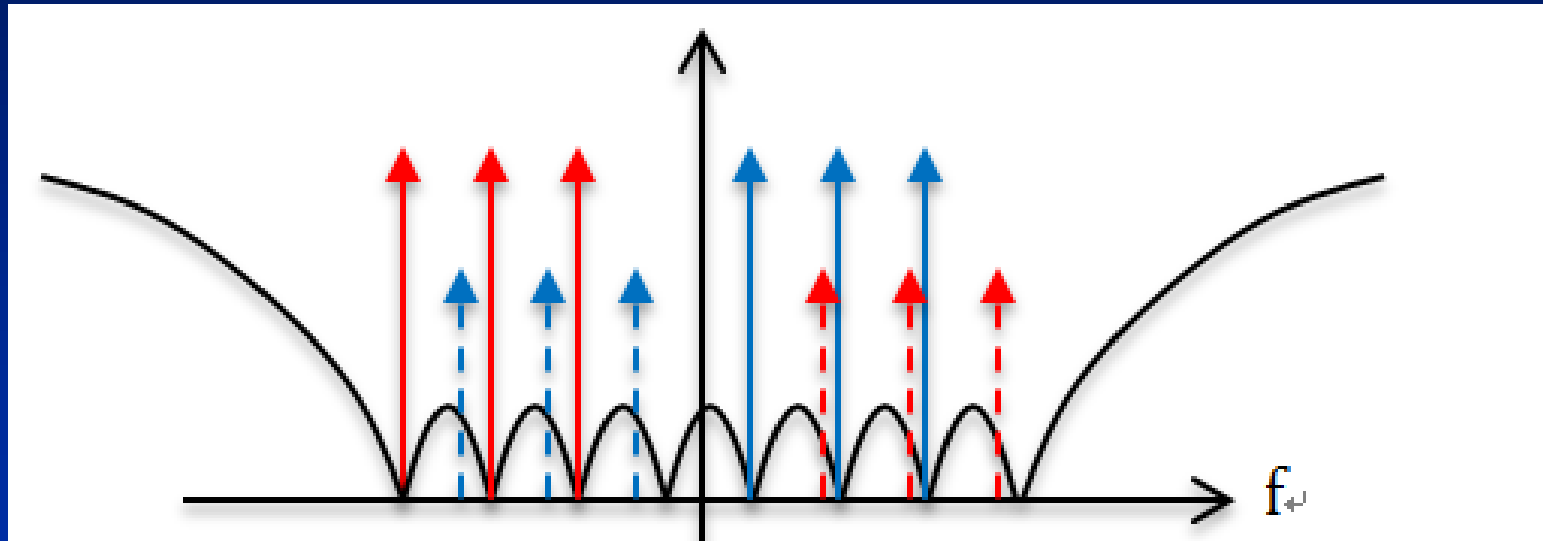
I-Q ADCs Testing



I-Q ADCs in receiver circuit

IC Testing with Complex Multi-tone Signal

Image Rejection Ratio Testing of Communication ICs



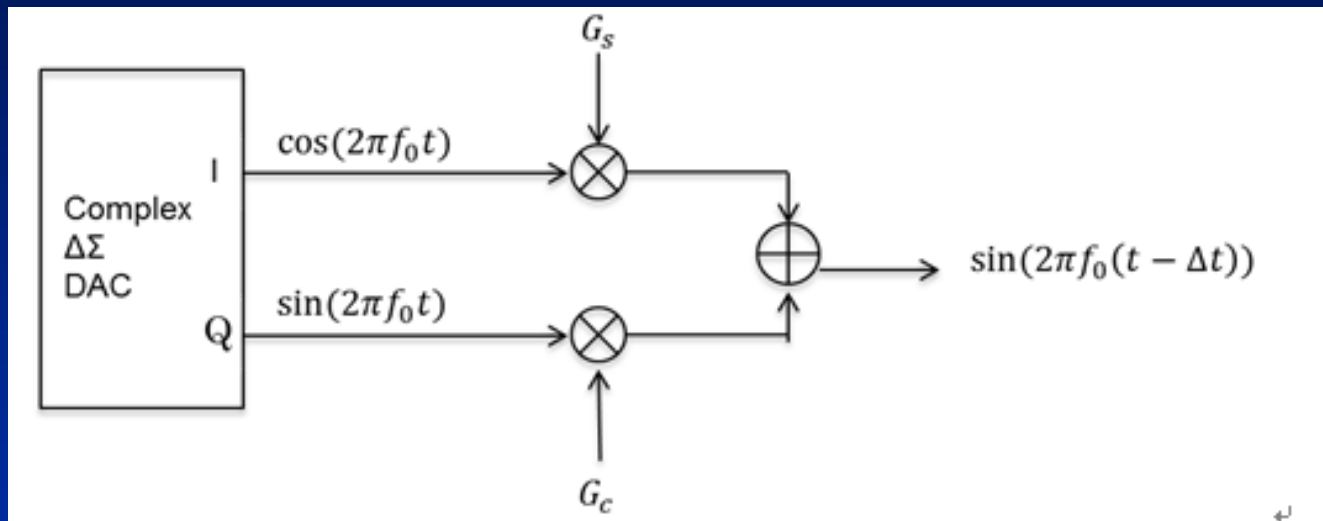
I, Q imbalance \rightarrow

Negative freq. (input) \rightarrow Positive freq. (output)

Suggested by an ATE vendor

IC Testing with Complex Signal

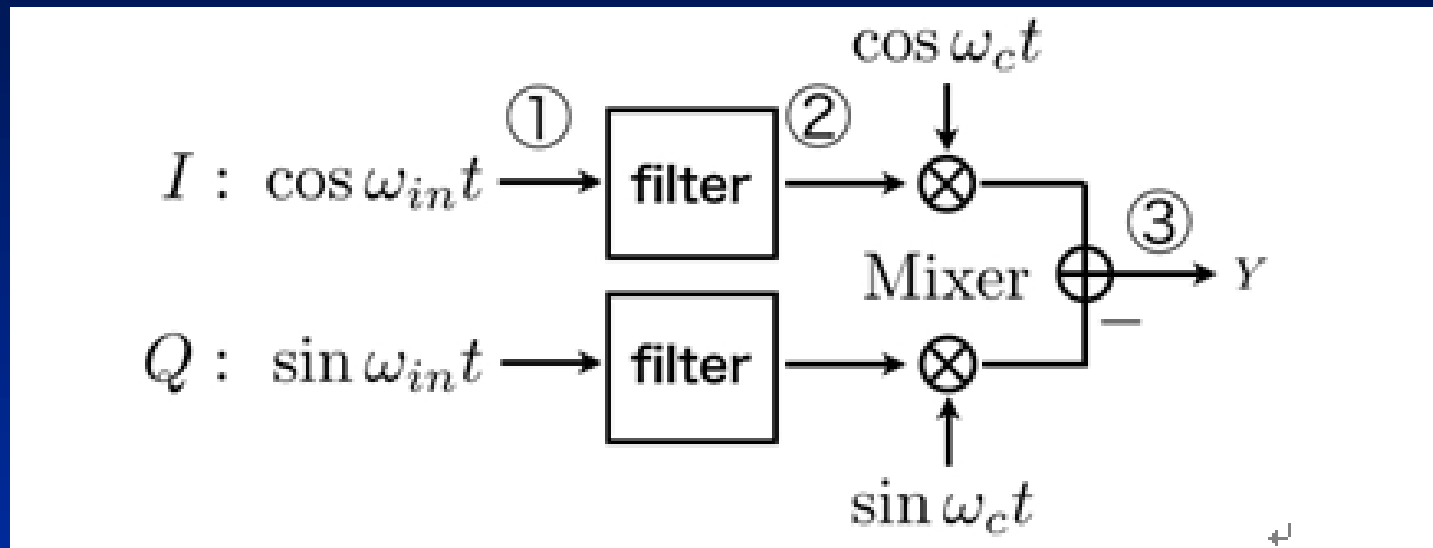
Clock phase fine adjustment system using complex signal



$$\begin{aligned} & \sin(2\pi f_0(t - \Delta t)) \\ &= \cos(2\pi f_0 \Delta t) \sin(2\pi f_0 t) - \sin(2\pi f_0 \Delta t) \cos(2\pi f_0 t) \\ &= G_C \sin(2\pi f_0 t) + G_S \cos(2\pi f_0 t) \end{aligned}$$

IC Testing with Complex Signal

High frequency signal generation



③

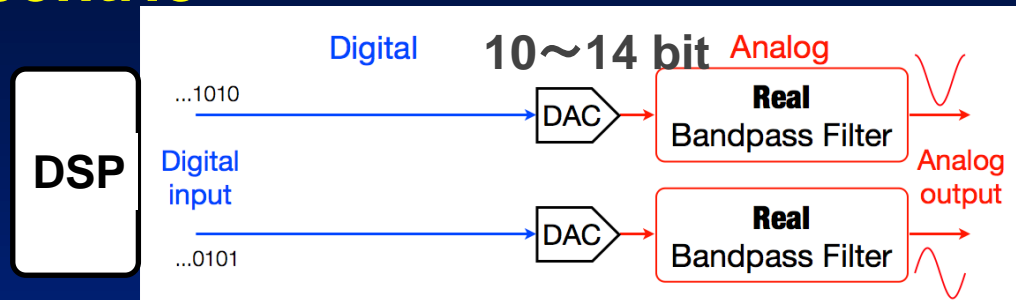
$$\begin{aligned} Y &= \cos \omega_{in} t \cdot \cos \omega_c t - \sin \omega_{in} t \cdot \sin \omega_c t \\ &= \cos(\omega_{in} + \omega_c) t \end{aligned}$$

Outline

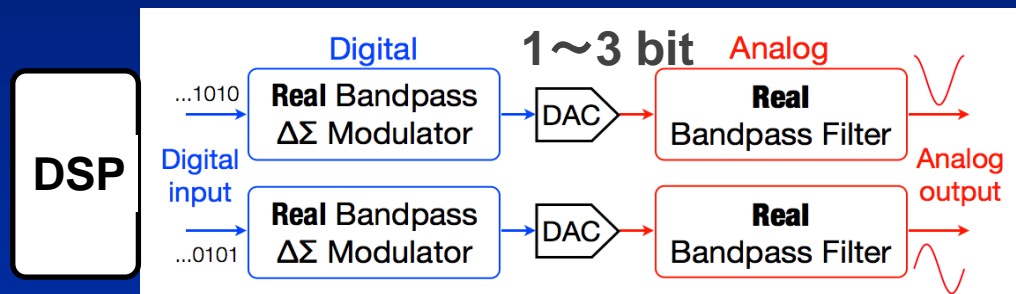
- Background to This Research
- Complex Multi-Band Signals
- **Complex Multi-BP $\Delta\Sigma$ DA Modulators**
- DWA Algorithm
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I,Q Signal Generation

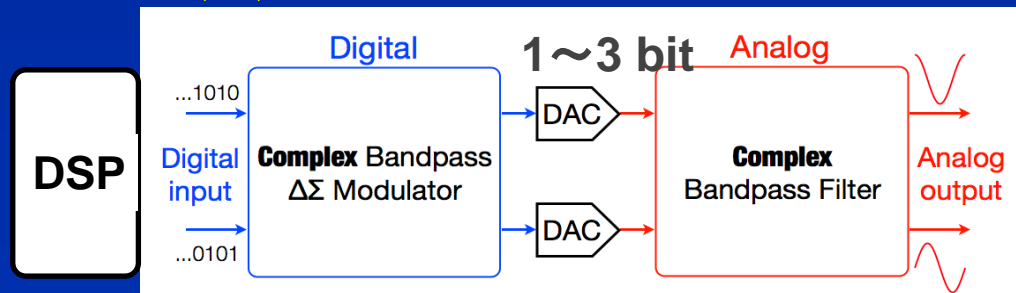
① Analog centric



② Digital centric(1)

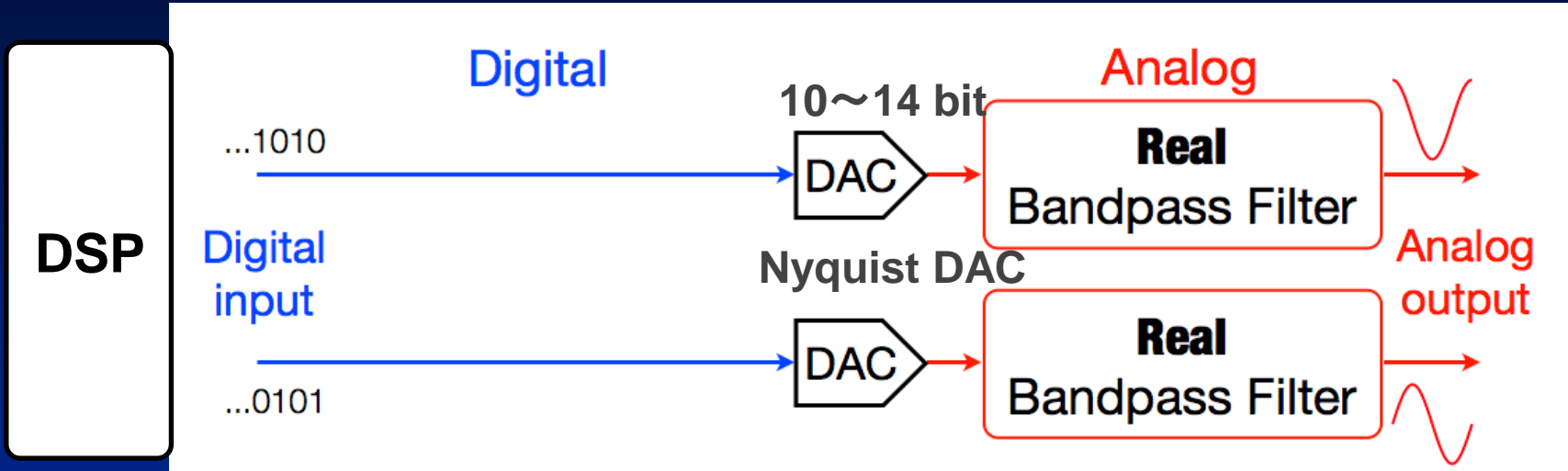


③ Digital centric(2)



Proposed

① Analog Centric

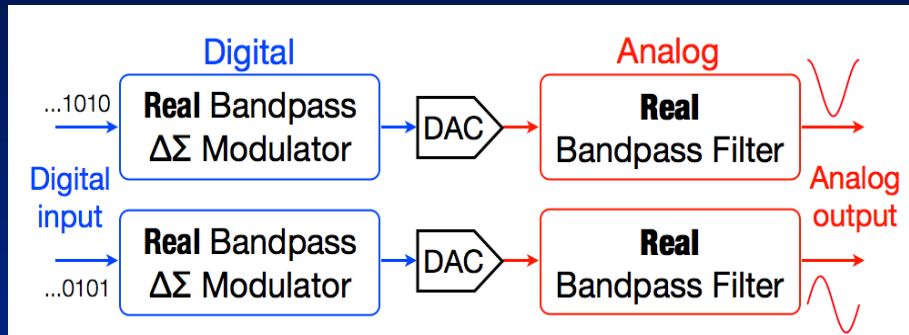


Large Nyquist-rate DACs
and
Steep analog filters

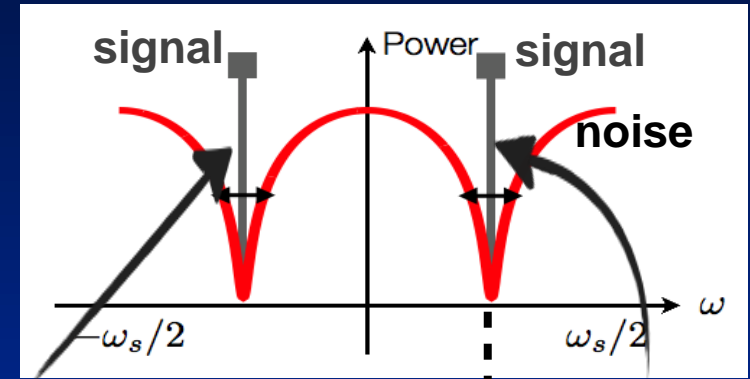
Delta Sigma DA Converter

Real vs Complex

② 2 Real-BP $\Delta\Sigma$ DACs



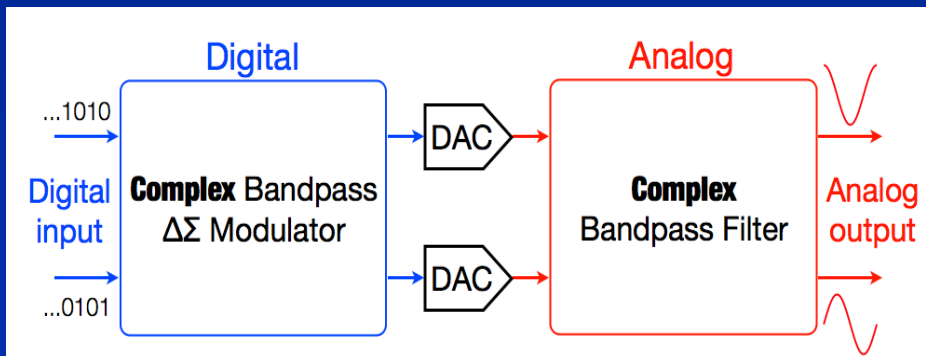
1~3 bit DAC



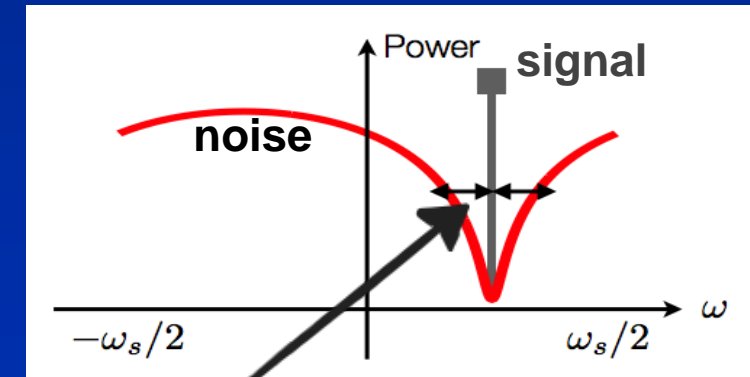
Unused band

Signal band

③ 1 Complex-BP $\Delta\Sigma$ DAC

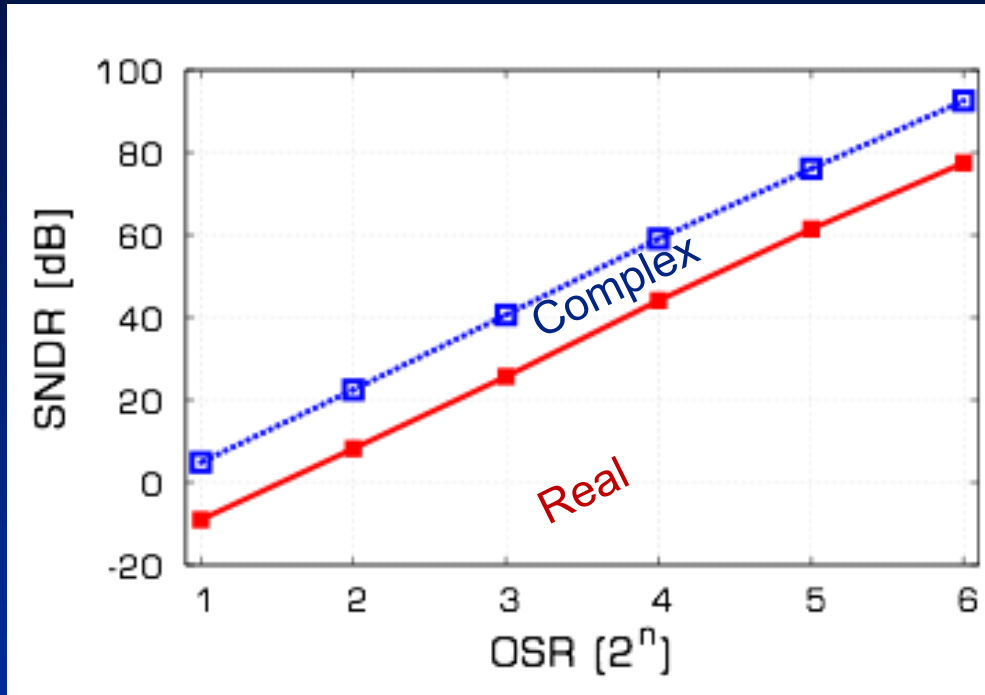


1~3 bit DAC



Wider signal band, High SNR

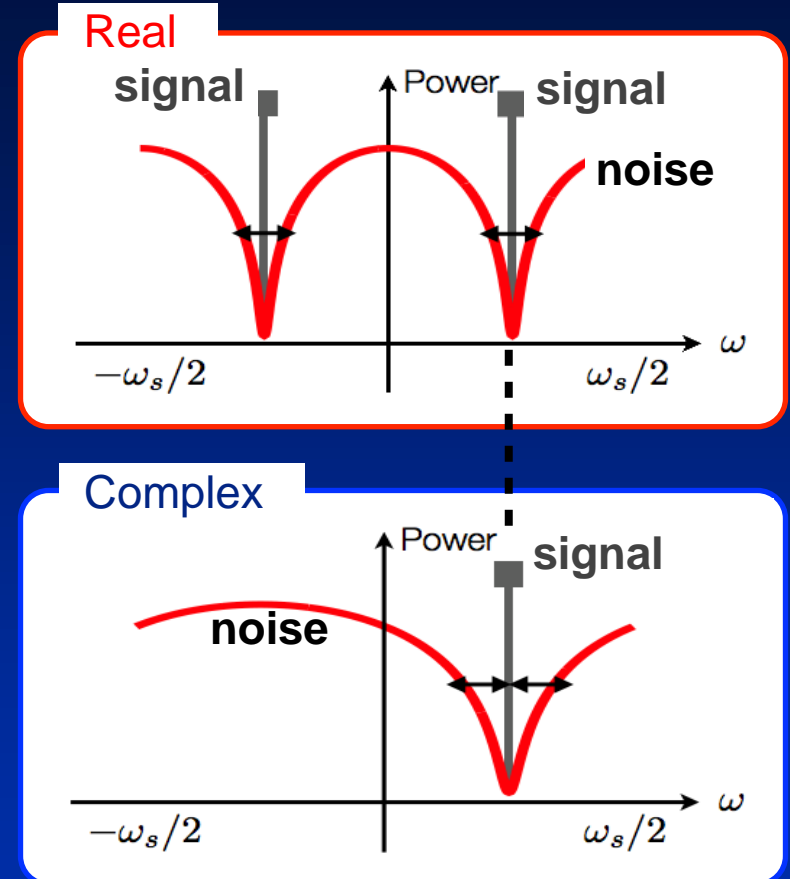
Complex Delta Sigma is Superior



OSR : Oversampling Ratio

15 dB better SNDR
for complex BP $\Delta\Sigma$ modulator

High quality I, Q signals



I,Q Signal Generation

DSP

+

$\Delta\Sigma$ DAC

+

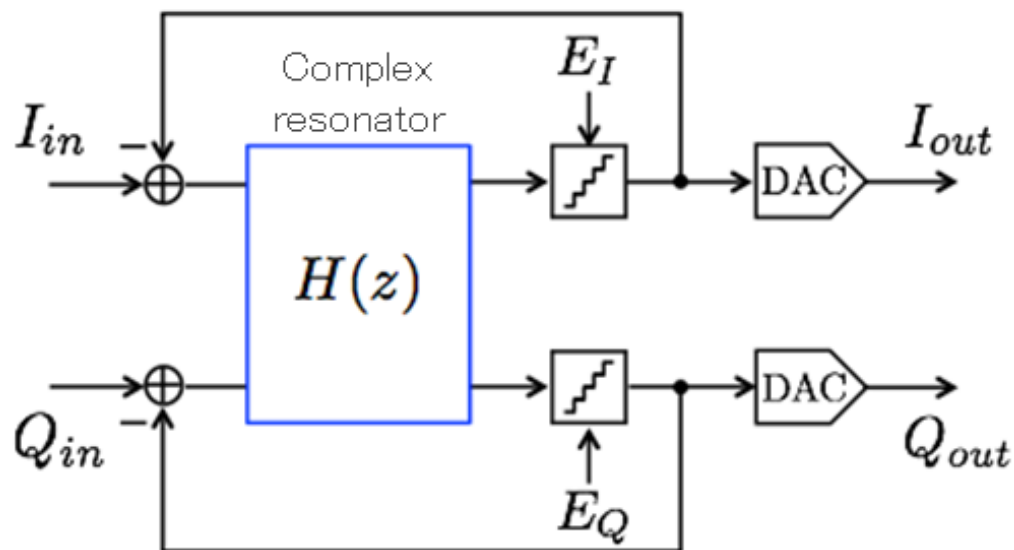
Complex

||

Low cost, high quality signal !

Digital rich !

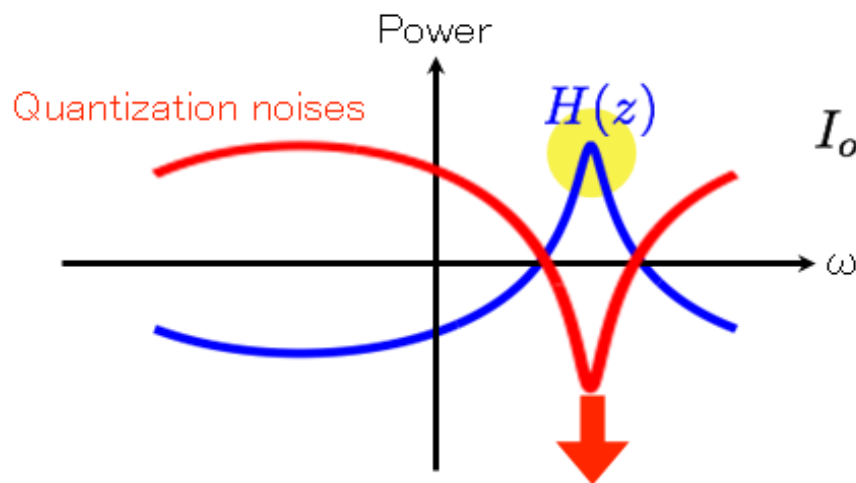
Principle of Complex BP Noise Shape



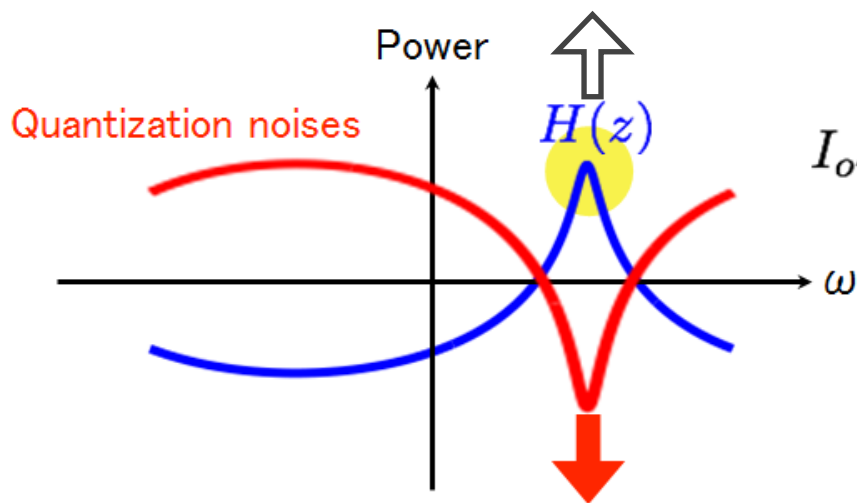
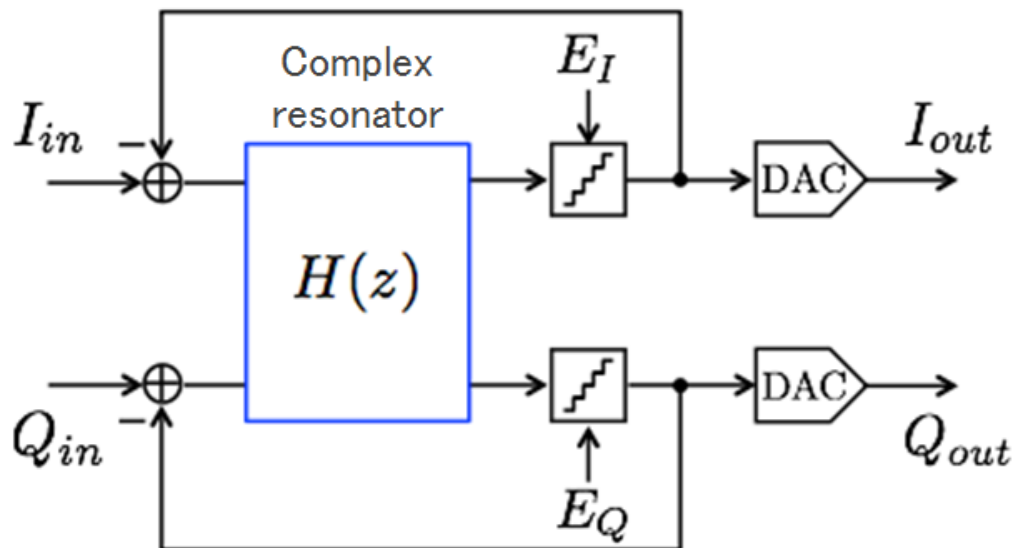
Signal Transfer Function

$$I_{out} + jQ_{out} = \frac{H(z)}{1 + H(z)} (I_{in} + jQ_{in}) + \frac{1}{1 + H(z)} (E_I + jE_Q)$$

Noise Transfer Function



Principle of Complex BP Noise Shape

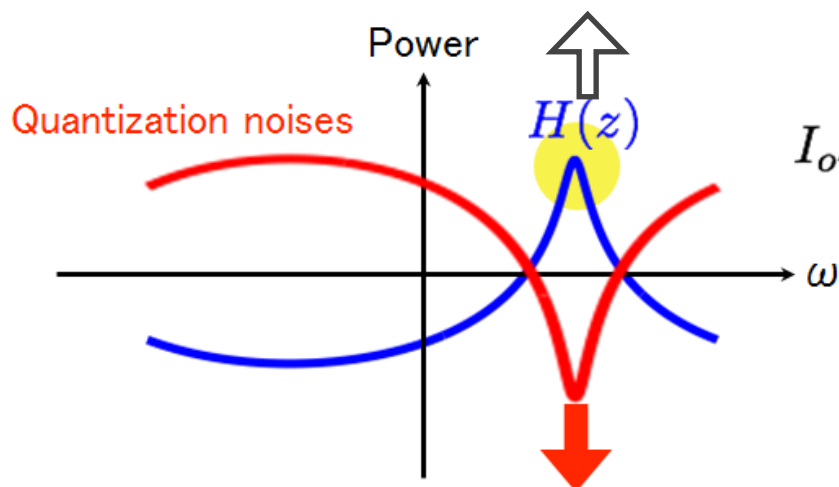
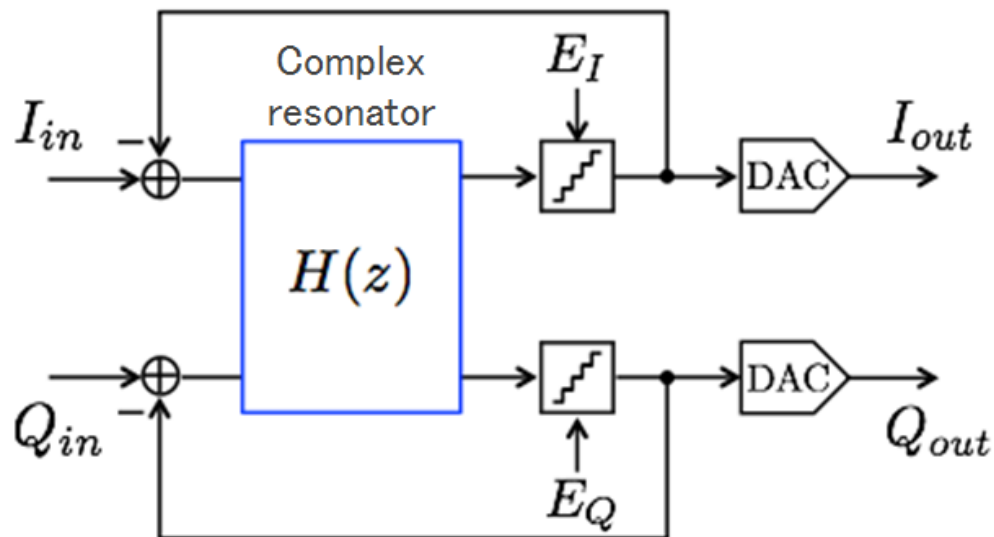


Signal Transfer Function = 1

$$I_{out} + jQ_{out} = \frac{\hat{H}(z)}{1 + \hat{H}(z)} (I_{in} + jQ_{in}) + \frac{1}{1 + \hat{H}(z)} (E_I + jE_Q)$$

Noise Transfer Function = 0

Principle of Complex BP Noise Shape

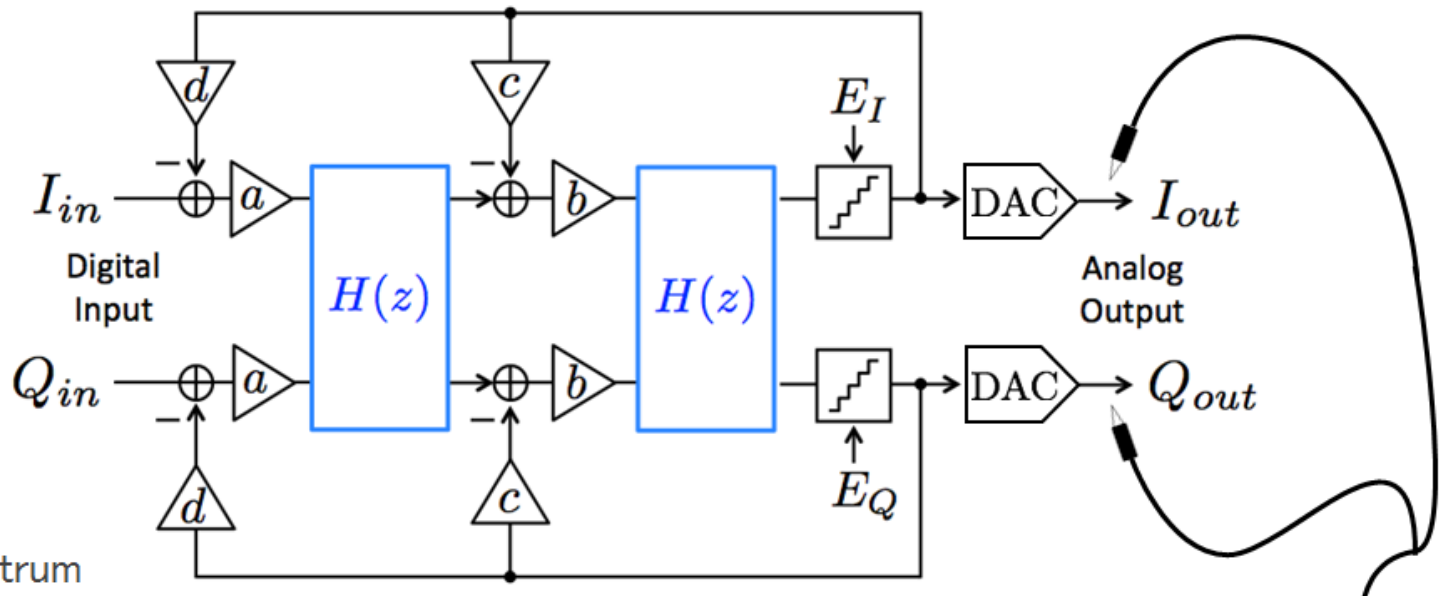


Signal Transfer Function = 1

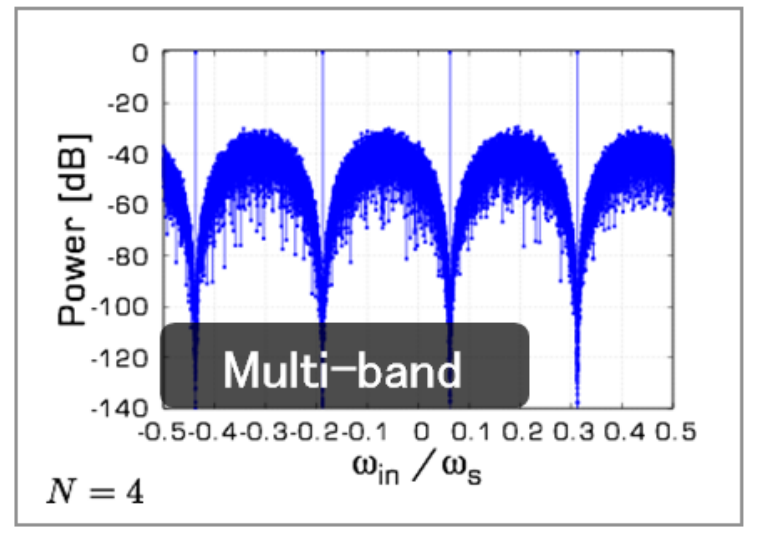
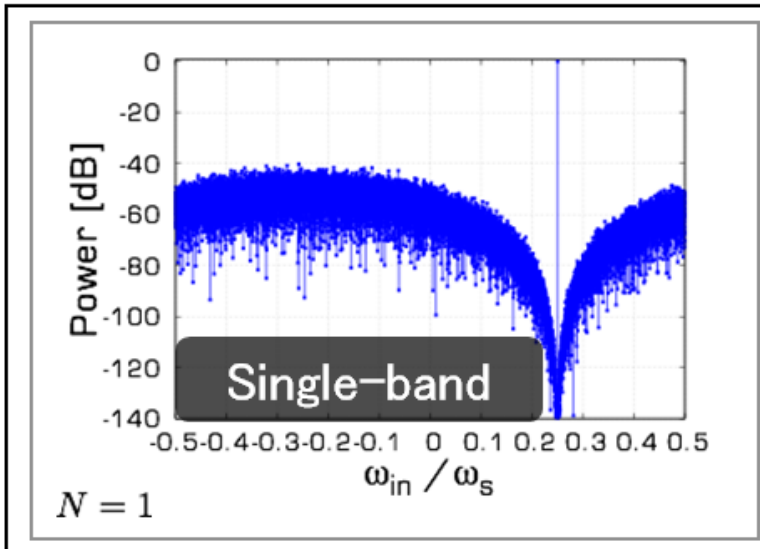
$$I_{out} + jQ_{out} = \boxed{1} (I_{in} + jQ_{in}) + \boxed{0} (E_I + jE_Q)$$

Noise Transfer Function = 0

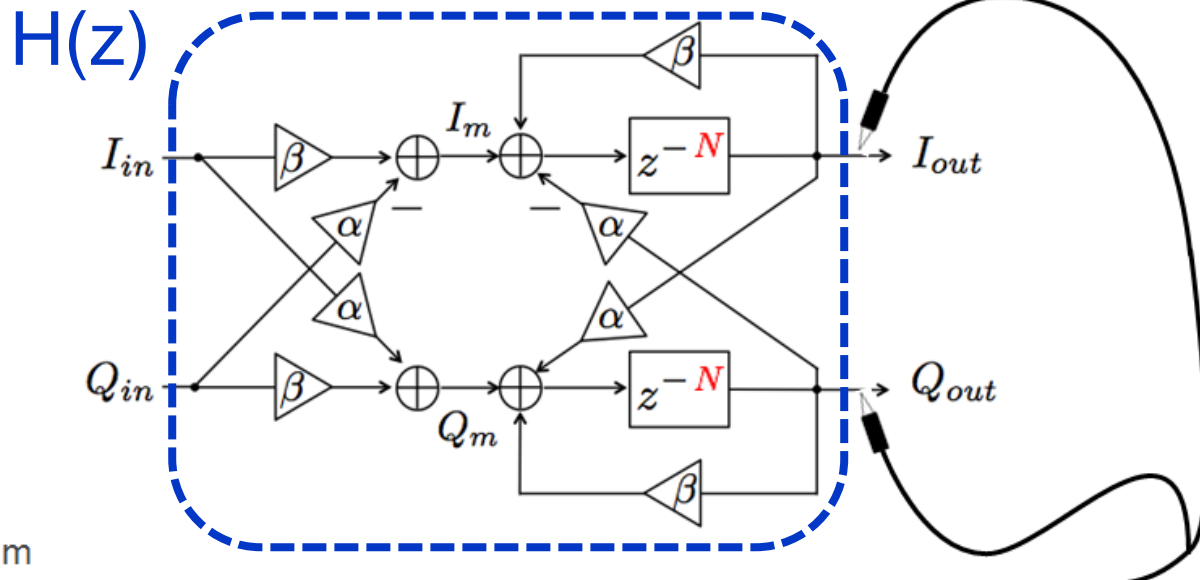
2nd-order Complex Multi-BP $\Delta\Sigma$ DAC



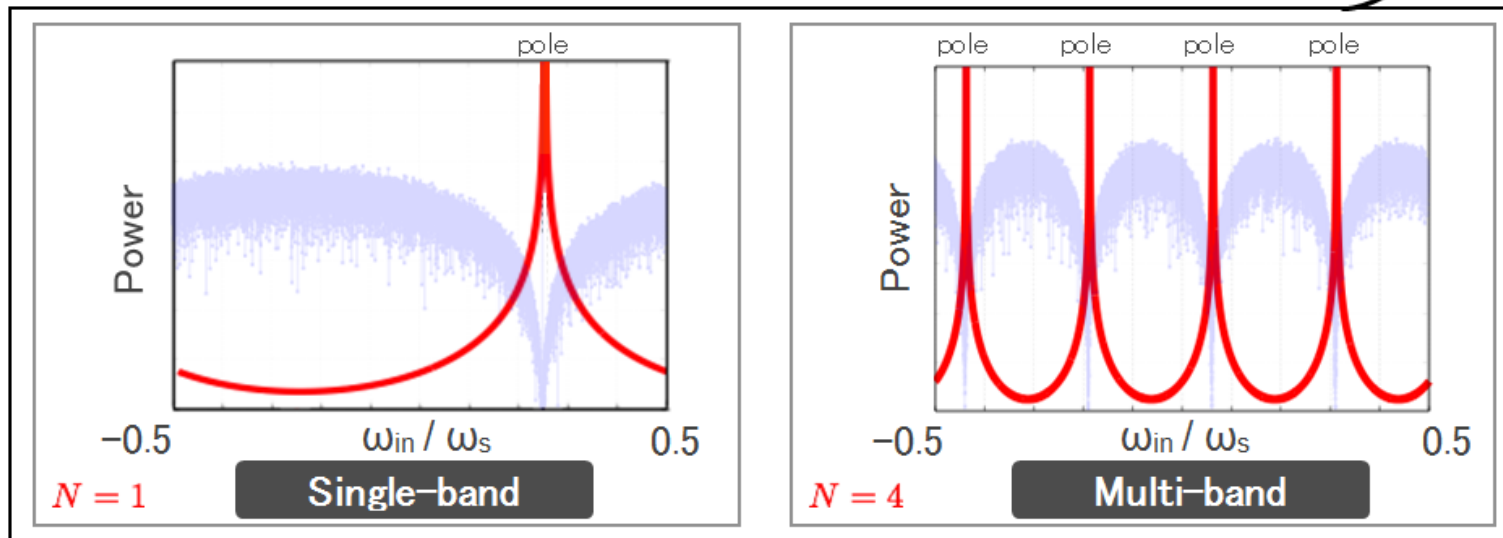
Output spectrum



Nth-order Complex Resonator



Output spectrum



Outline

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- Complex Multi-Band Signals
- Complex Multi-BP $\Delta\Sigma$ DA Modulators
- DWA Algorithm

DWA: Data Weighted Averaging

One of
Dynamic Element Matching (DEM) algorithms

Multi-bit DA Modulator

Multi-bit DA modulator (2~3bit)

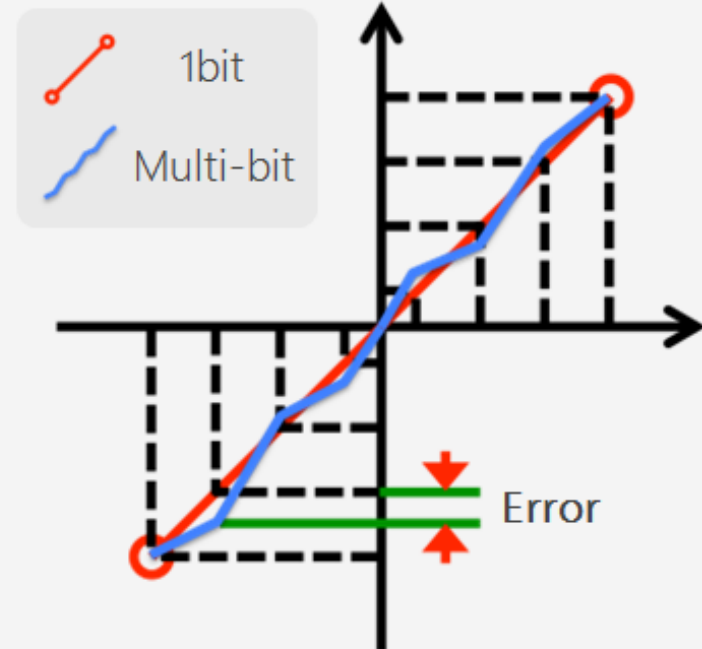
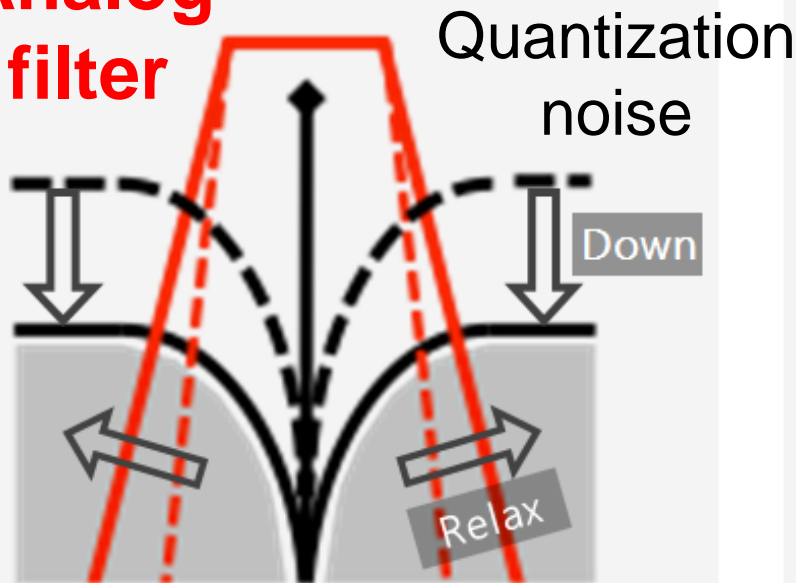


Quantization noise reduction

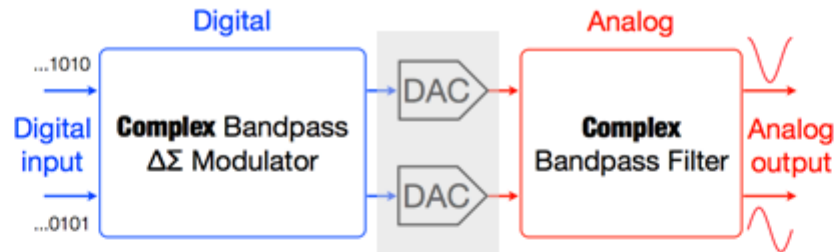


Linearity degradation

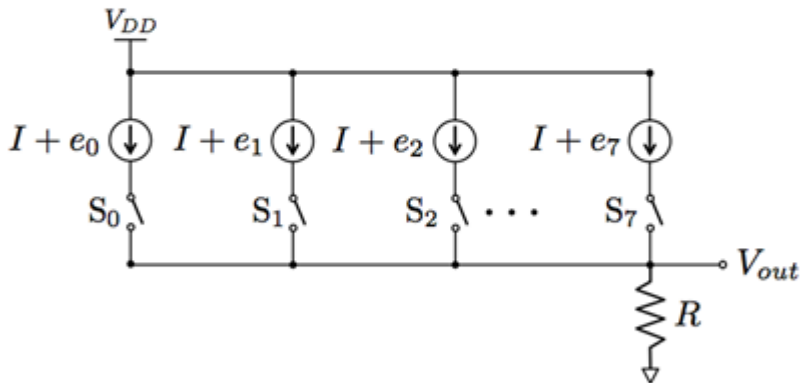
Analog filter



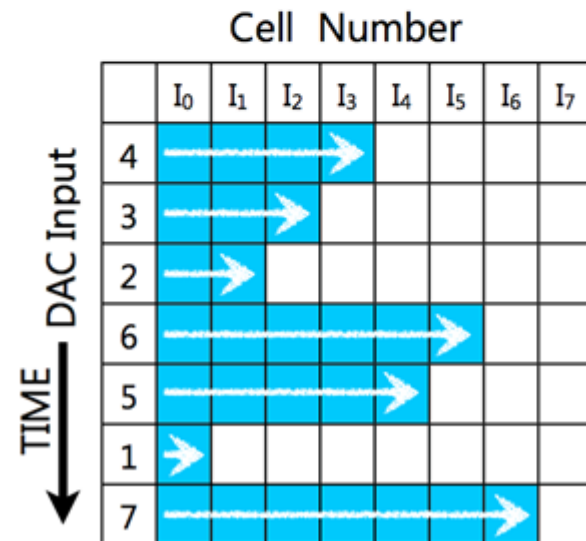
Multi-bit DAC



Normal unary DAC



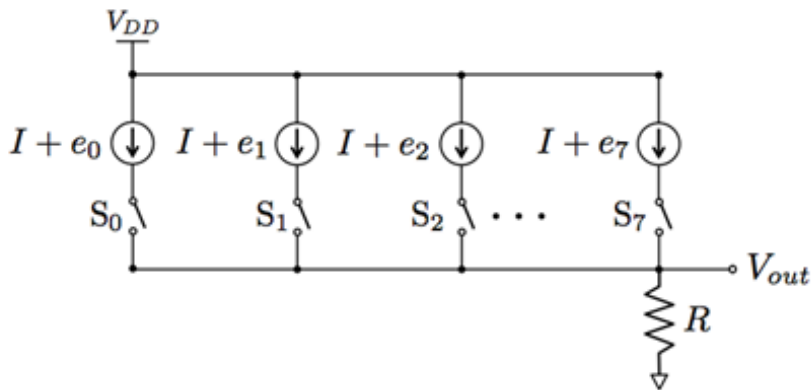
e_i : current source mismatch



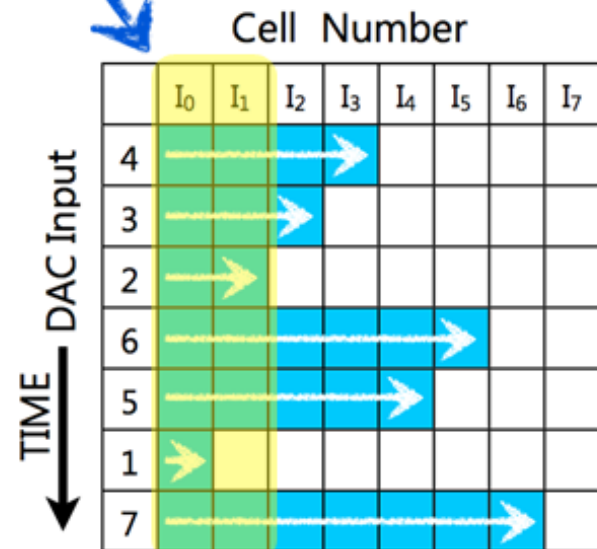
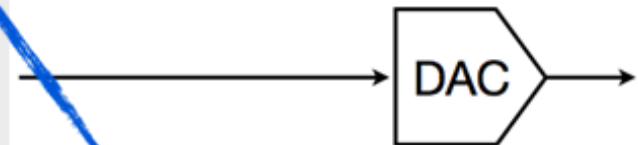
Multi-bit DAC

Accumulate mismatch of particular cell

Normal unary DAC



e_i : current source mismatch

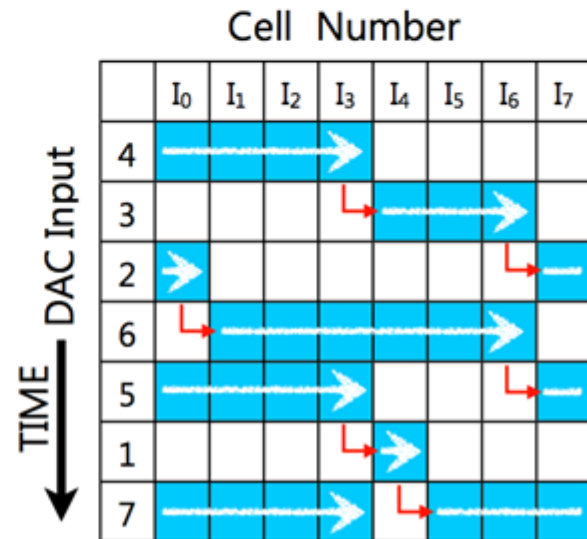
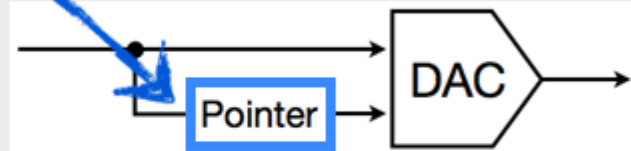
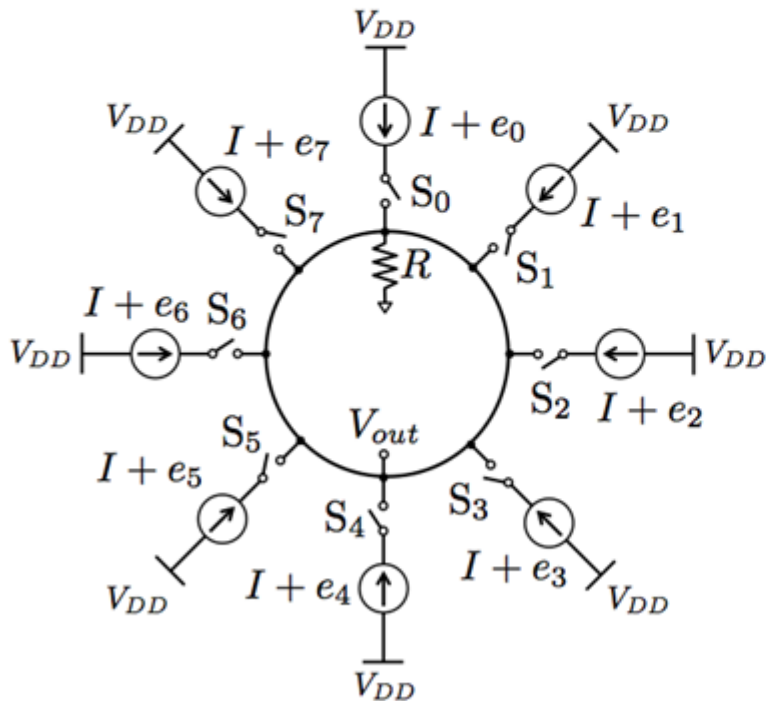


Multi-bit DAC + DWA

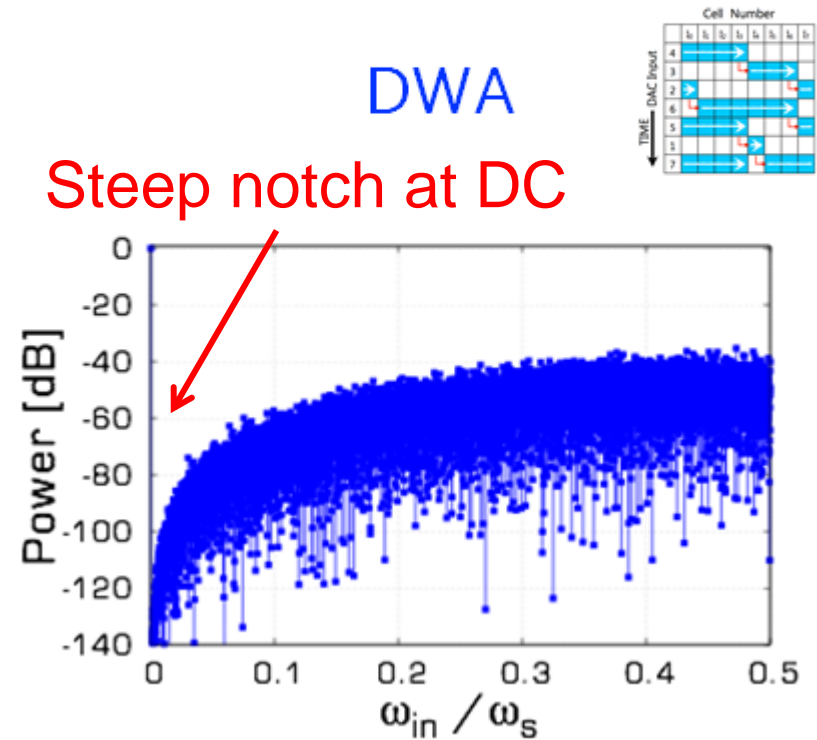
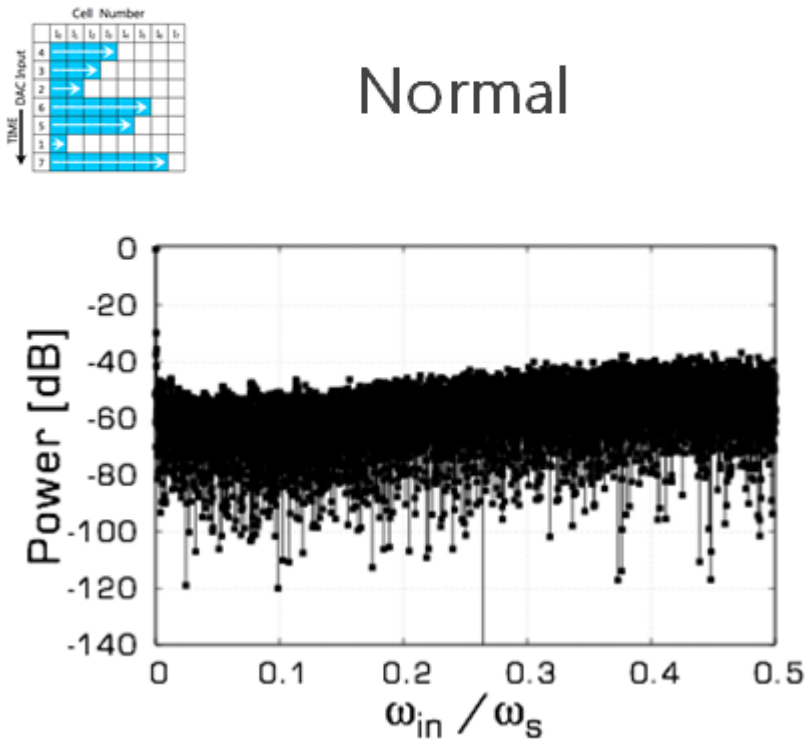
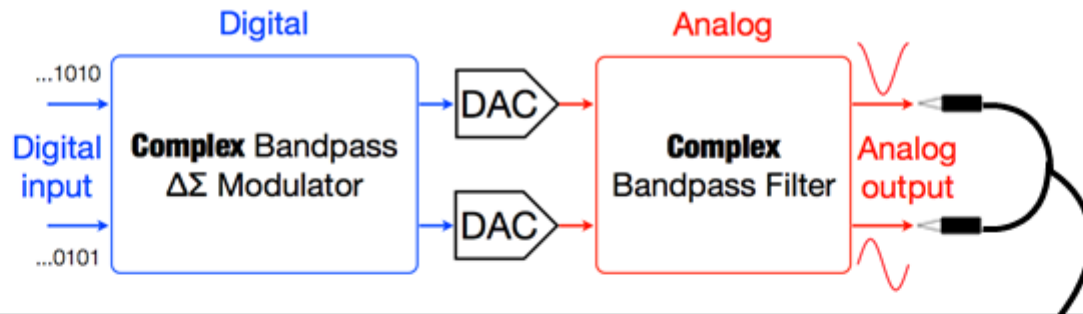
Memorize next cell selection start point

DWA* DAC

*Data Weighted Averaging | Select the element with DSP algorithm



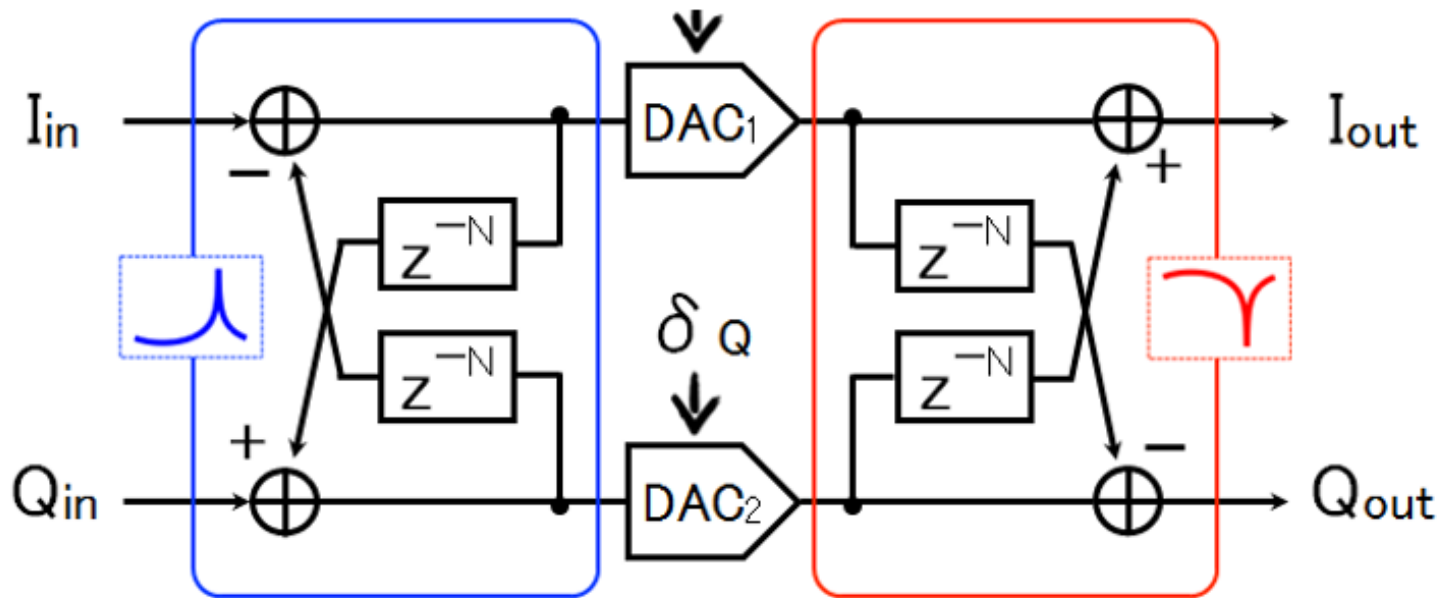
Effect of DWA




Equivalent Circuit of Complex DWA

Complex resonator

Complex notch



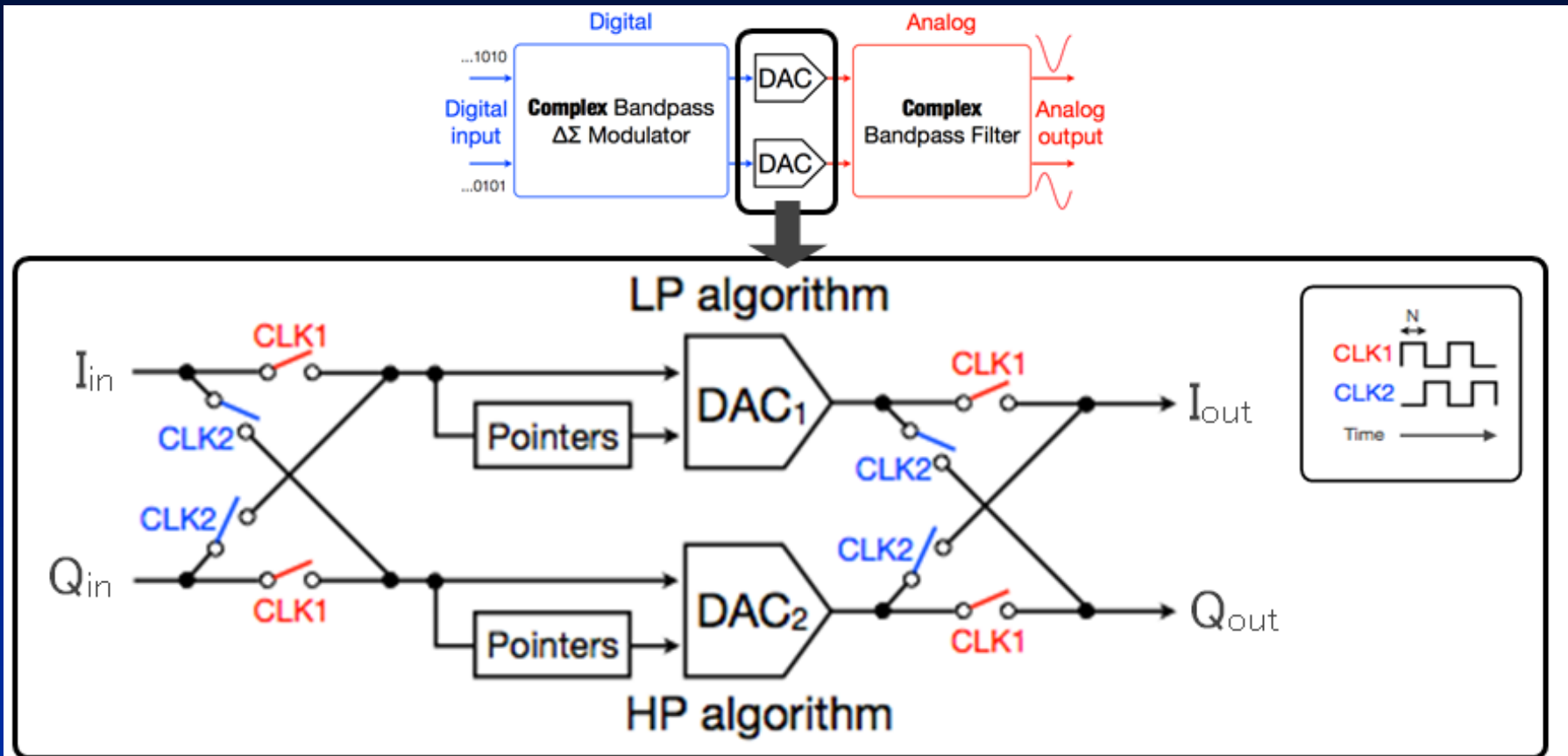
δ_I, δ_Q affected by only complex notch

DAC input can be ∞ 



Can't be realized directly

Equivalent Circuit Implementation

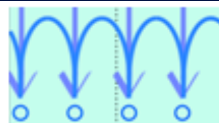


- ◆ Attach pointers
- ◆ Exchange upper-path and lower-path every N clock

➔ **Complex DWA is realized.**

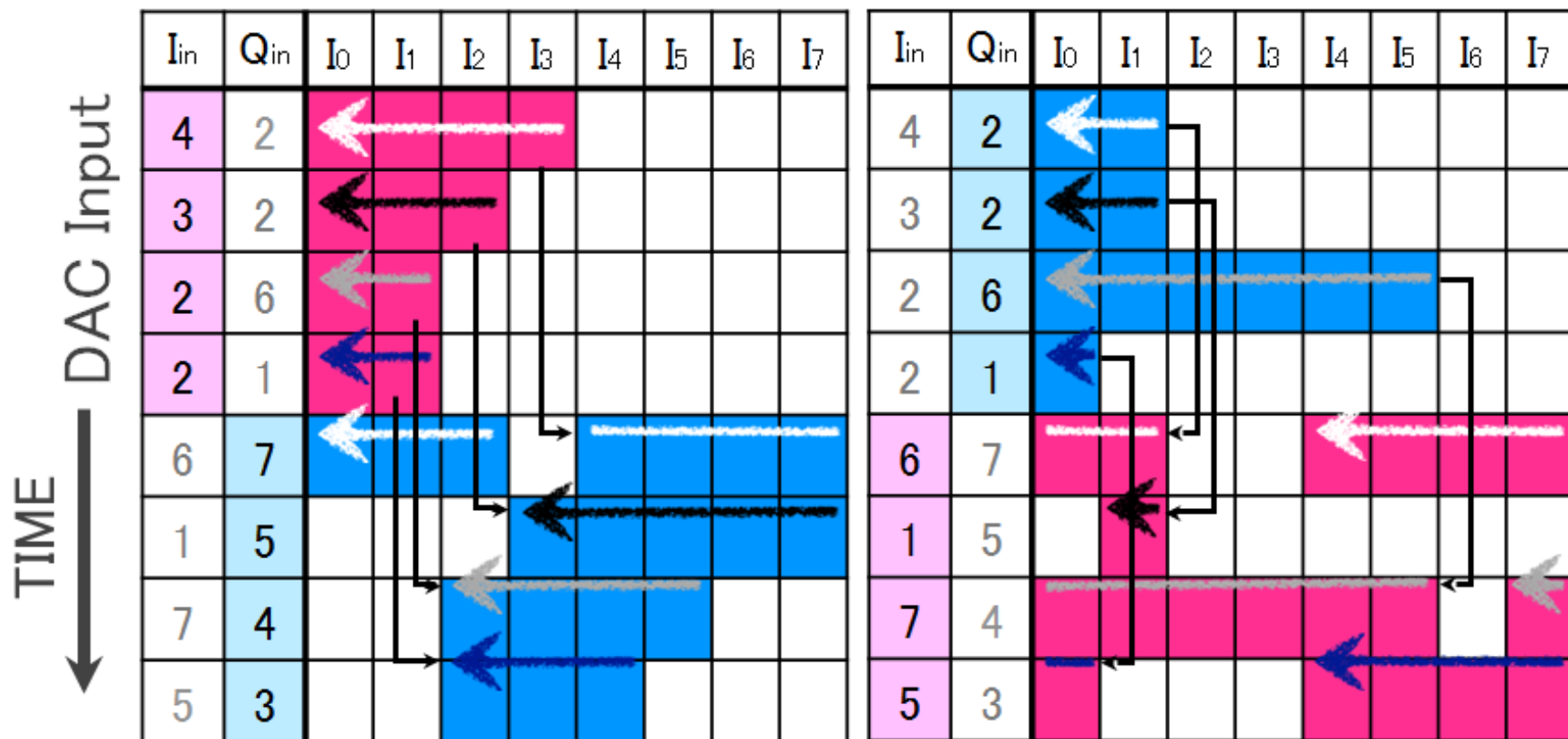
Complex Multi-Bandpass DWA Algorithm

$N = 4$ (four zero points)

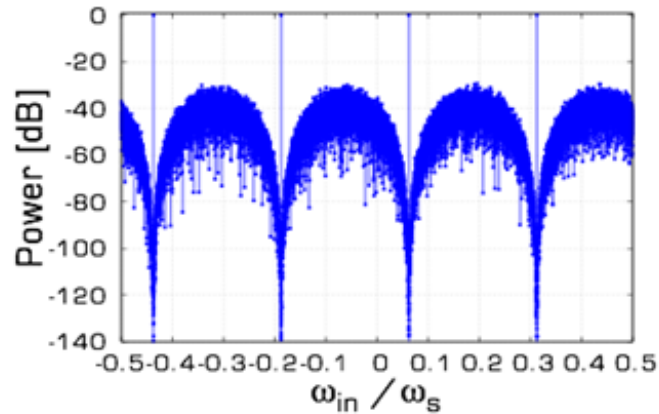
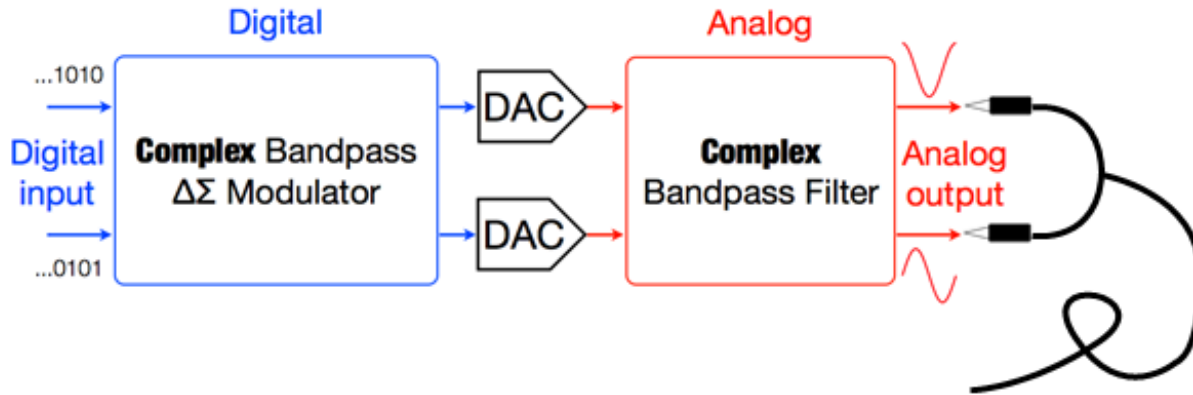


DAC₁ (LP operation)

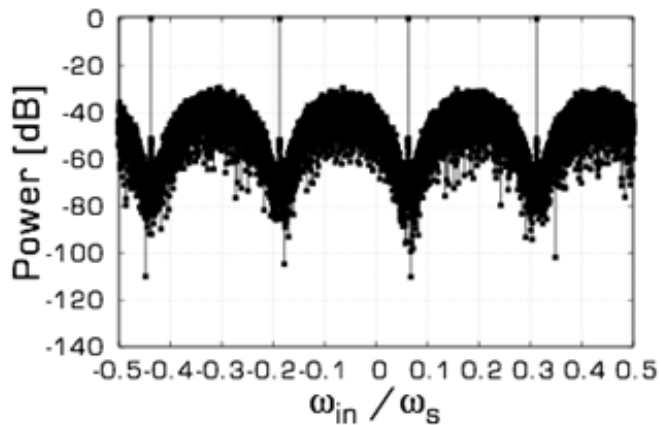
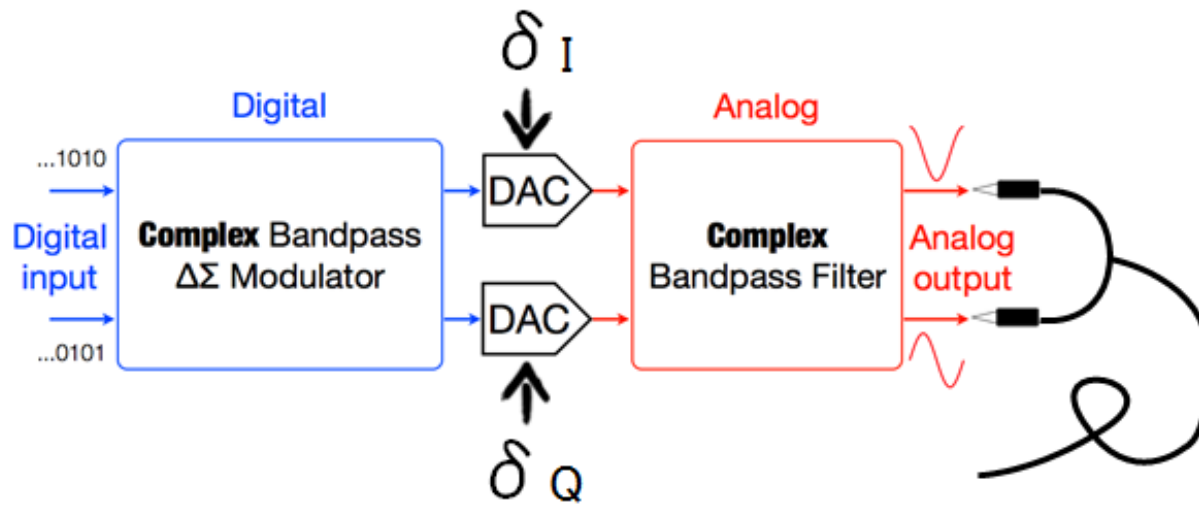
DAC₂ (HP operation)



Simulation Result ~Ideal Linear DAC~



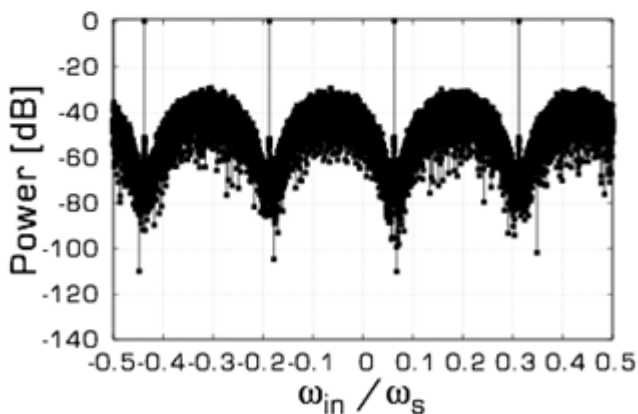
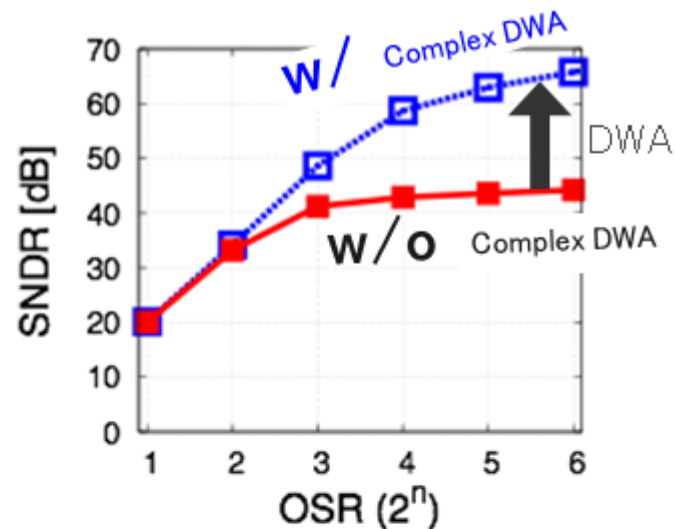
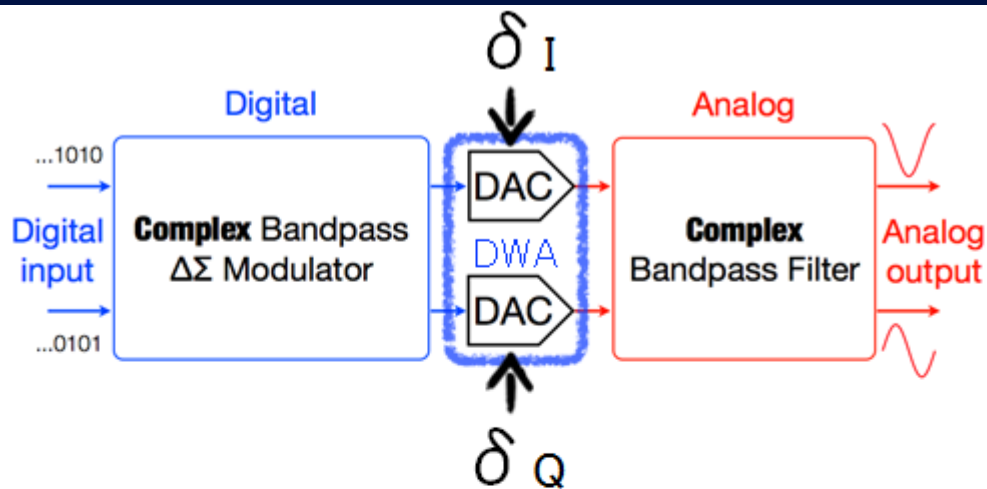
Simulation Result ~Actual Nonlinear DAC~



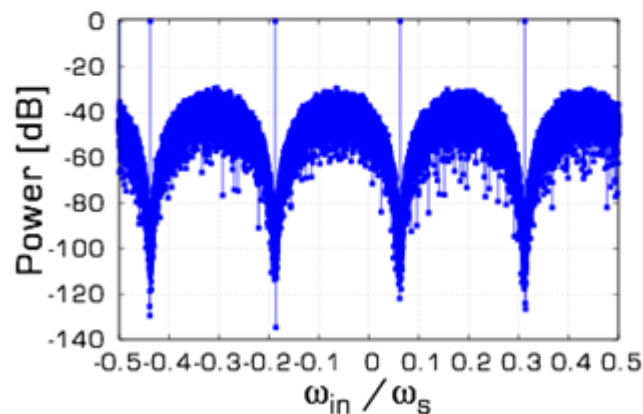
Notches filled with noise

Simulation Result

~ Actual Nonlinear DAC + DWA ~



DWA



Notches filled with noise



Steep Notches

Outline

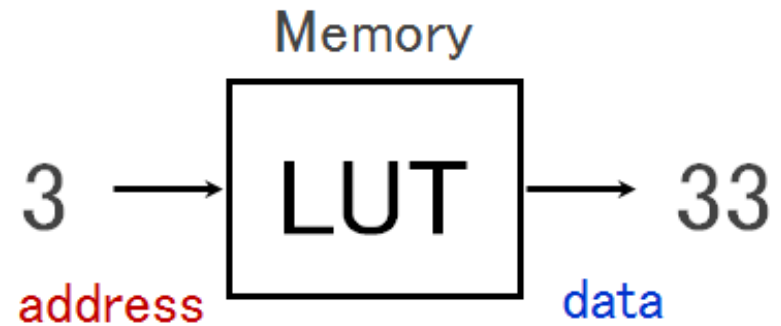
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Look Up Table

Example



Cat Age	Human Age
1	20
2	27
3	33
4	39
5	45
6	50
7	55
8	60

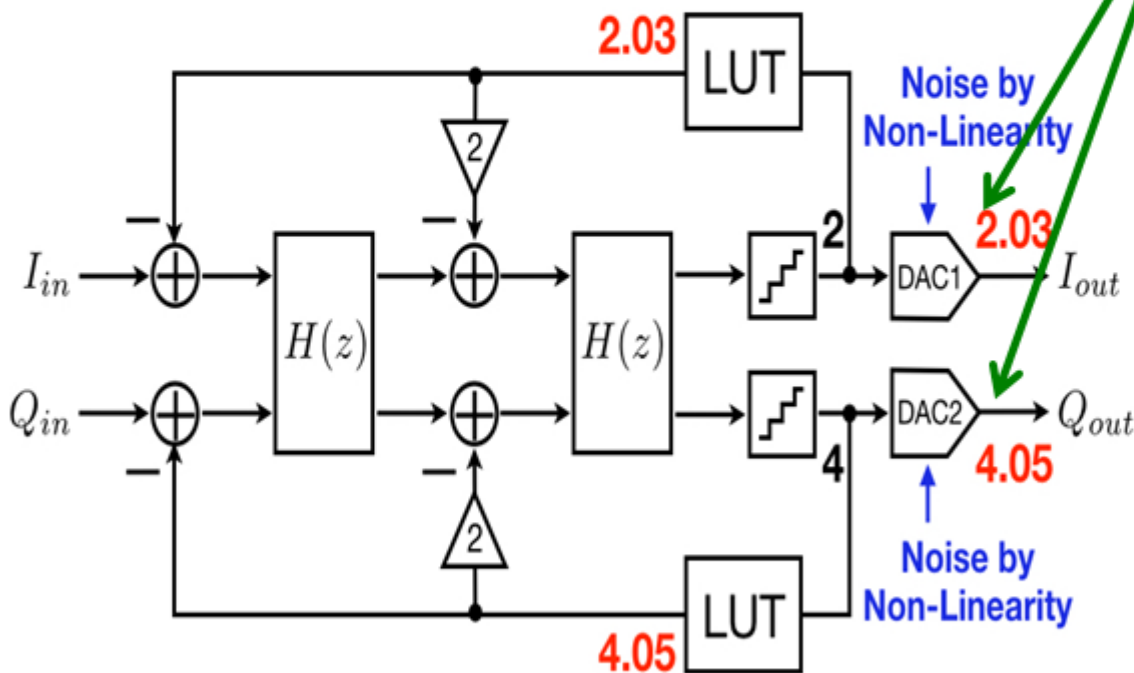


DAC Nonlinearity Measurement

Results are stored in LUTs

$\Delta \Sigma$ ADC
inside SoC

2nd Complex Multi-BP $\Delta \Sigma$ DA Modu. + Non-Linear DAC

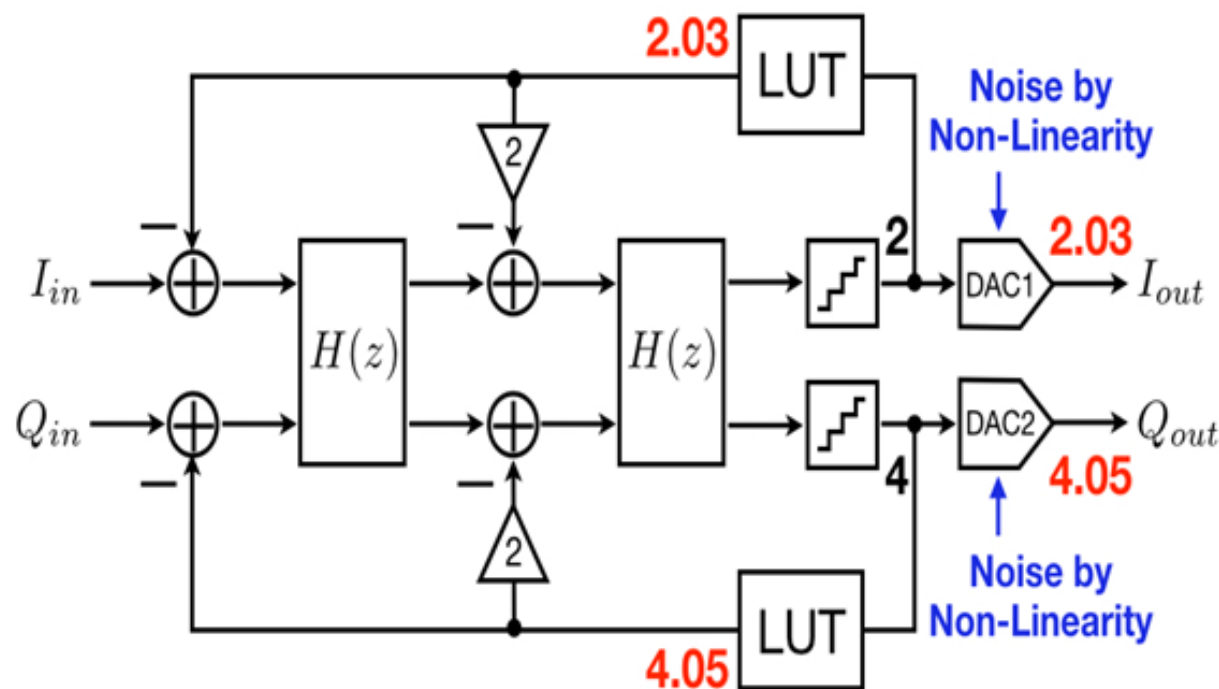


LUT

Address	I	Q
0		
1		
2	2.03	
3		
4		4.05
...		

$\Delta\Sigma$ DAC with Self-Calibration of DAC1, DAC2

CLK(1)

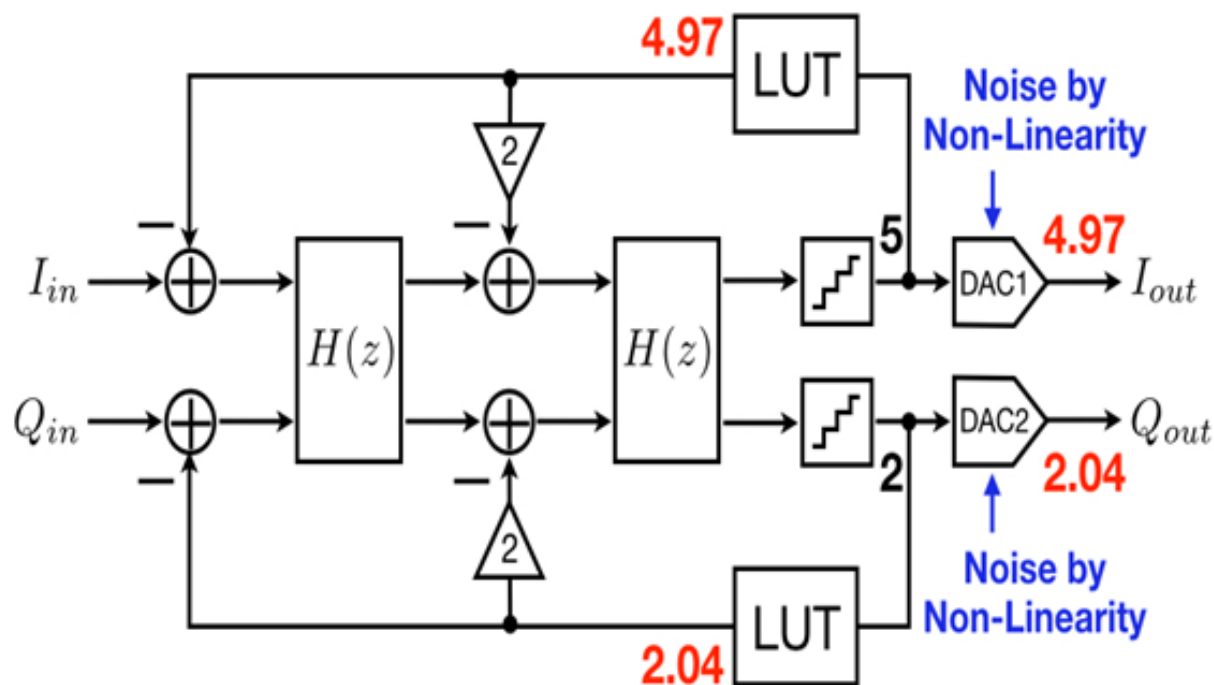


LUT

Address	I	Q
0	0.00	0.00
1	1.05	0.97
2	2.03	2.04
3	2.99	3.01
4	4.02	4.05
...		

$\Delta\Sigma$ DAC with Self-Calibration of DAC1, DAC2

CLK(2)

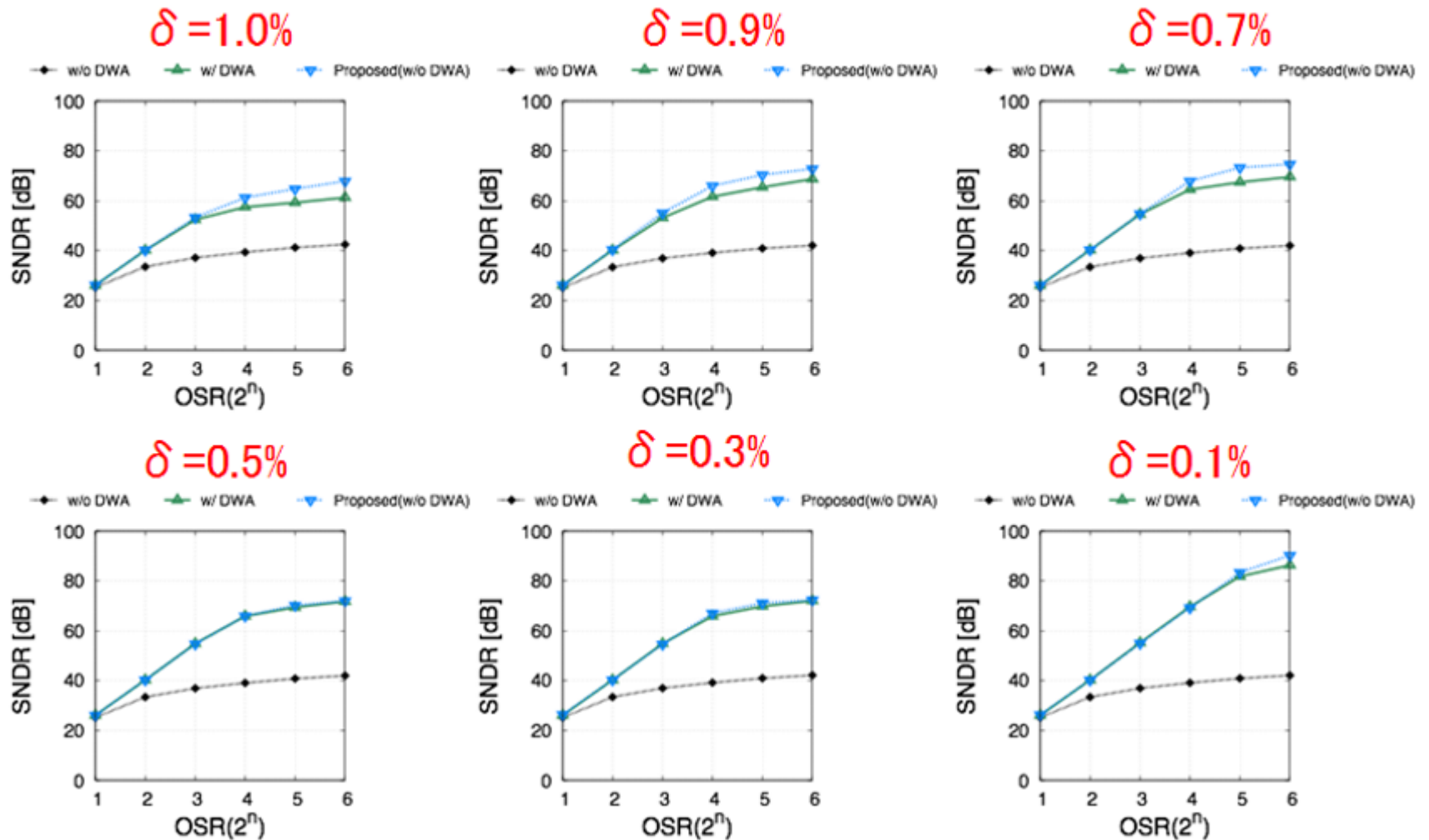


LUT

Address	I	Q
0	0.00	0.00
1	1.05	0.97
2	2.03	2.04
⋮		
5	4.97	5.03
⋮		

Simulation Results

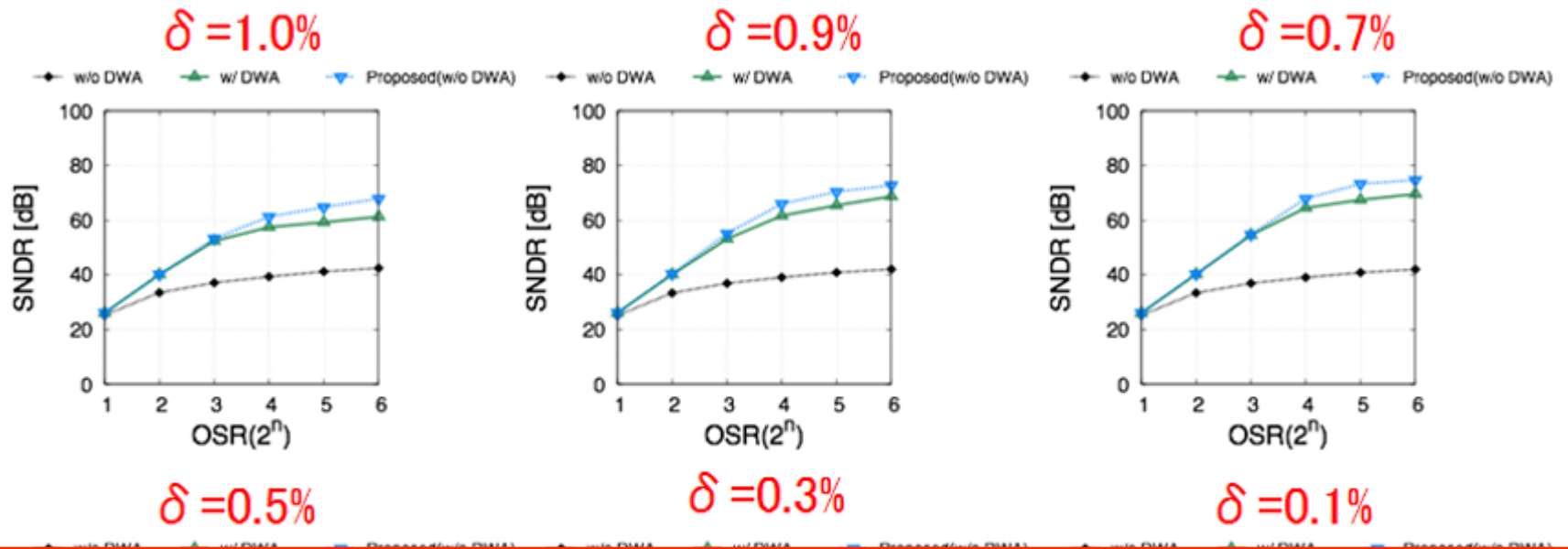
Simulation Conditions



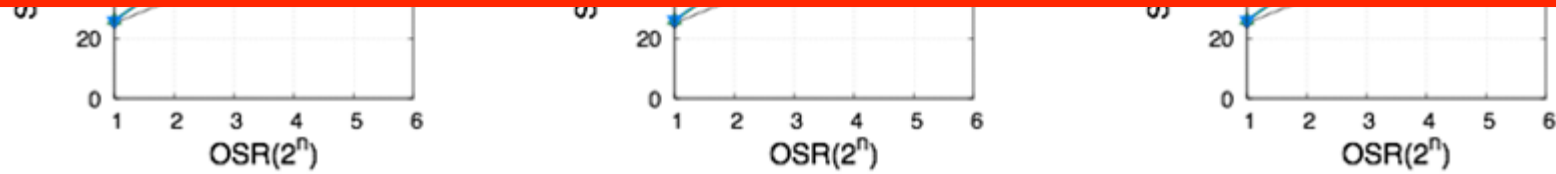
Simulation Results

Simulation Conditions

① **w/o DWA** ② **w/ DWA** ③ **Self-calibration**



When DAC nonlinearity is large, **self-calibration (③)** is more effective than **DWA (②)**.



Pros and Cons of Self-Calibration

Pros

	DWA	Self-Calibration
DAC Nonlinearity Noise Shaping	Specific Bands	All Bands

- Better SNDR than DWA is obtained.

Cons

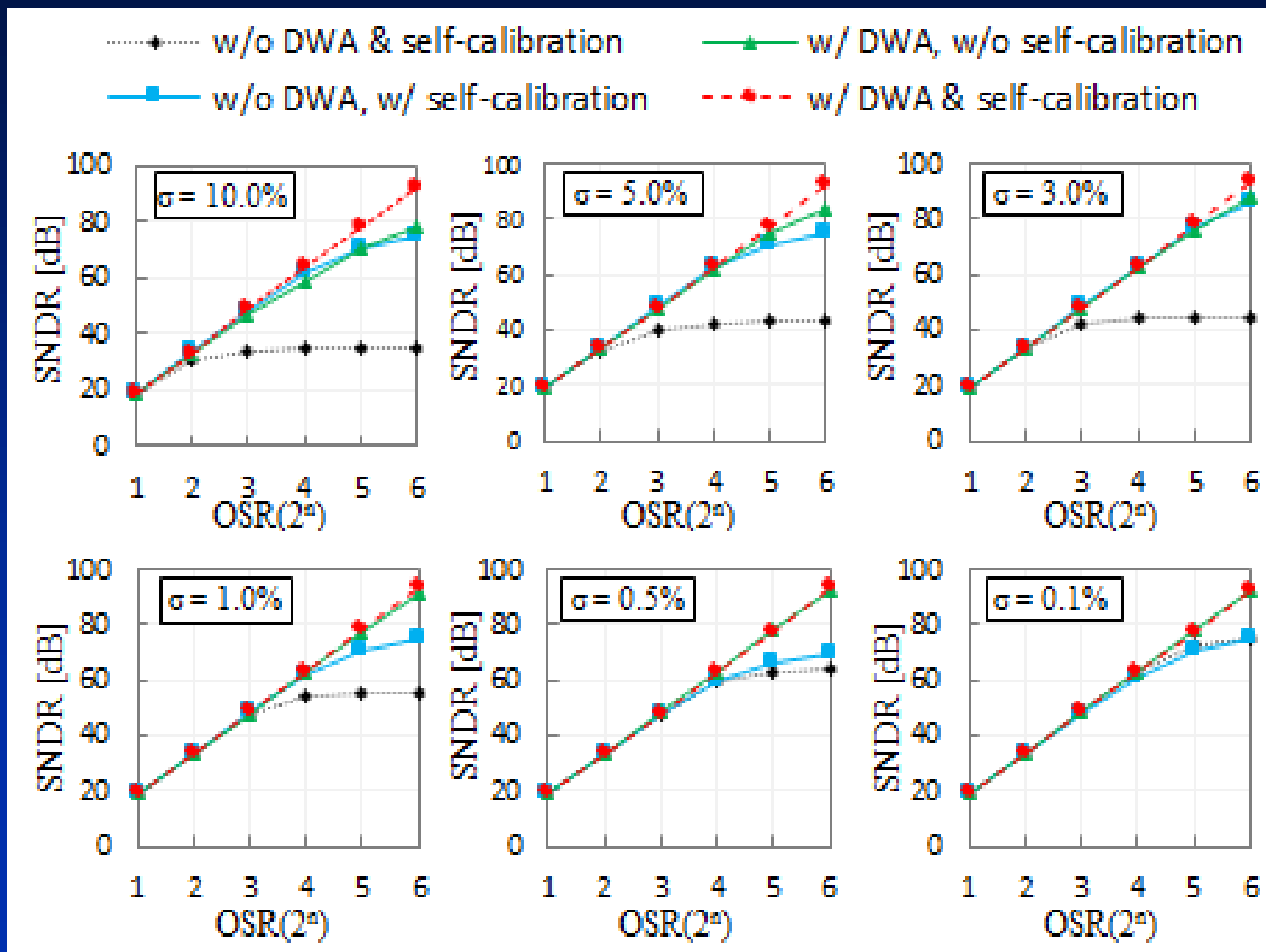
- DAC nonlinearity measurement with delta-sigma ADC is required.

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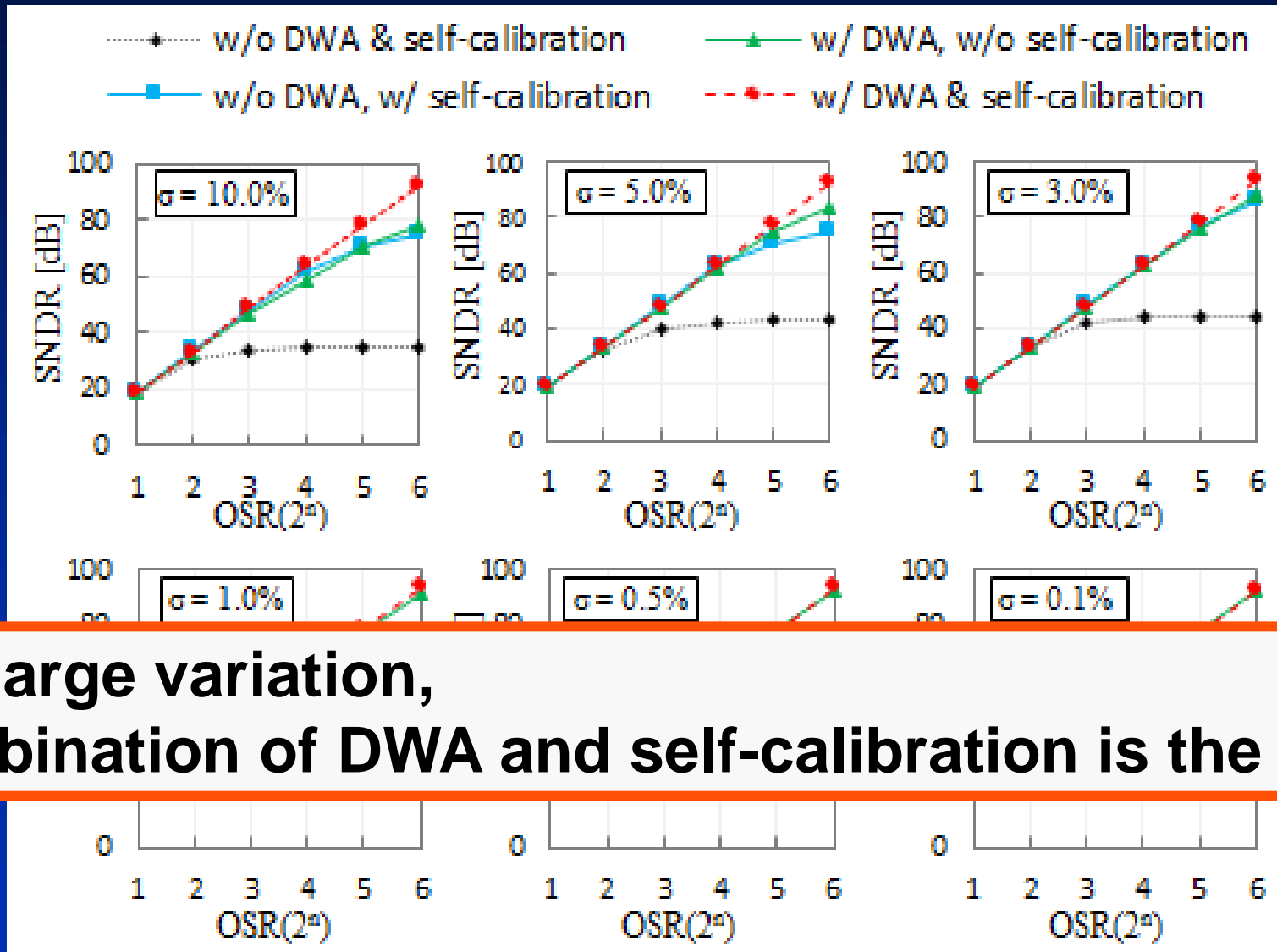
Combination of DWA and Self-Calibration

LP case



Combination of DWA and Self-Calibration

LP case



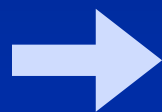
For large variation, combination of DWA and self-calibration is the best.

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- Conclusions

Conclusion

- I-Q signal generation with digital centric
- Complex multi-BP $\Delta\Sigma$ DAC
- Multi-bit DAC
 - Relaxes analog filter requirements
 - x Degrades system linearity

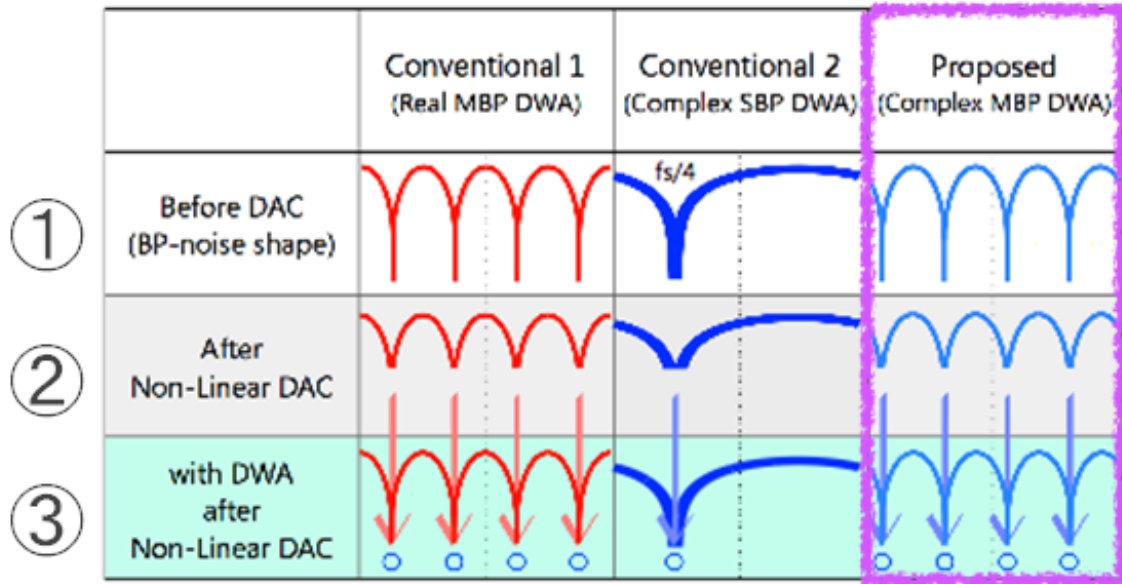


DWA algorithm
Self-calibration algorithm
Their combination

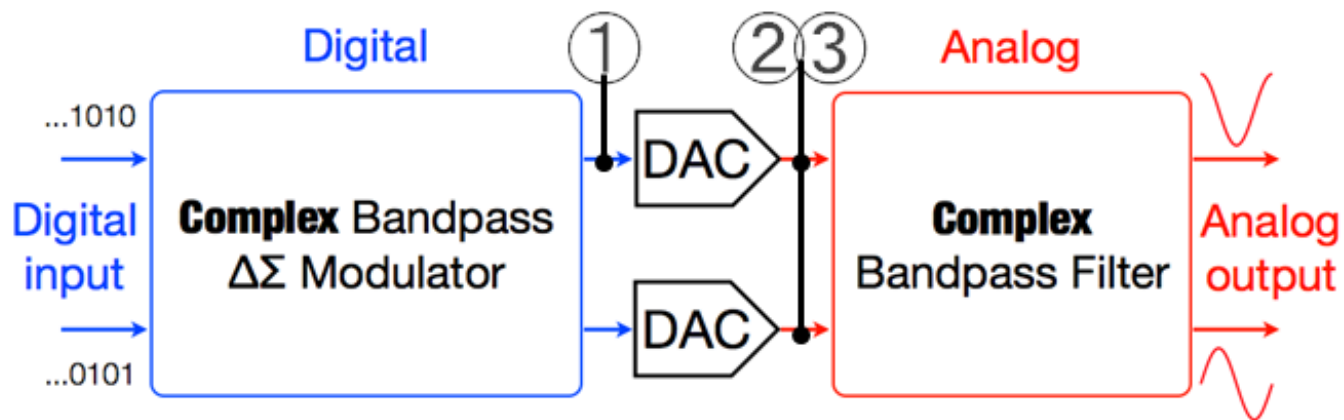
Low cost, high quality I-Q signal generation.

Back Up

Type of DWA

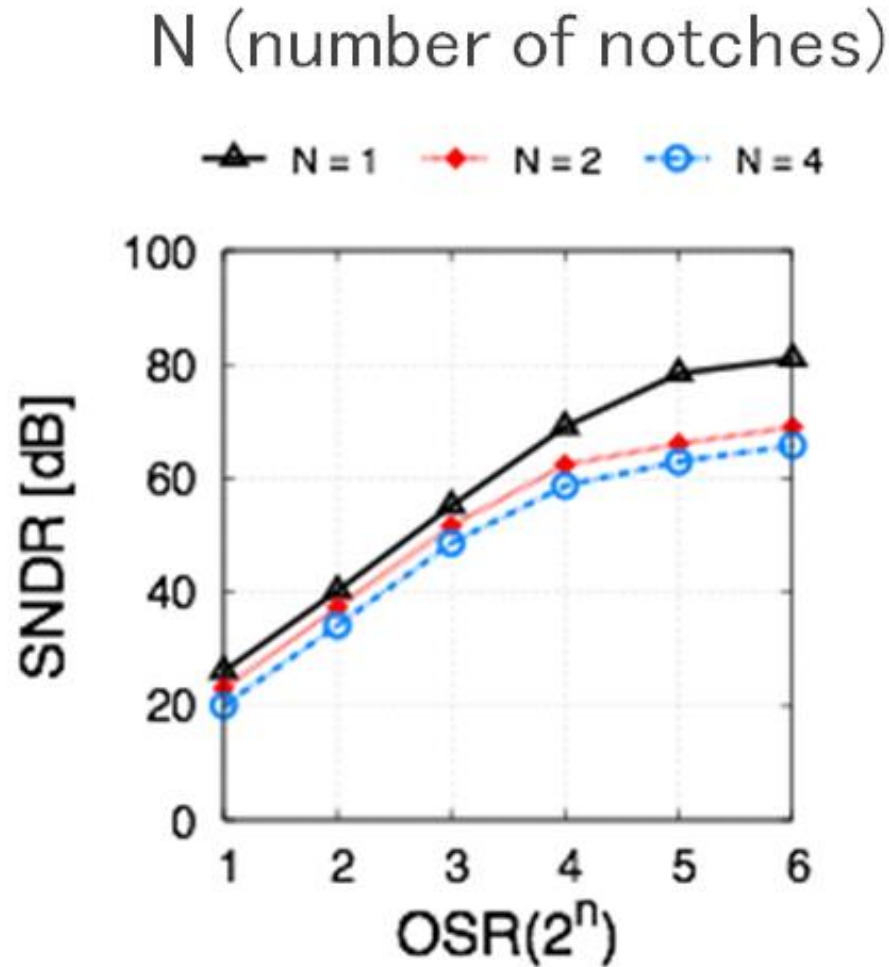


DWA
||
DSP algorithm



Simulation Result

~ Actual Nonlinear DAC + DWA ~

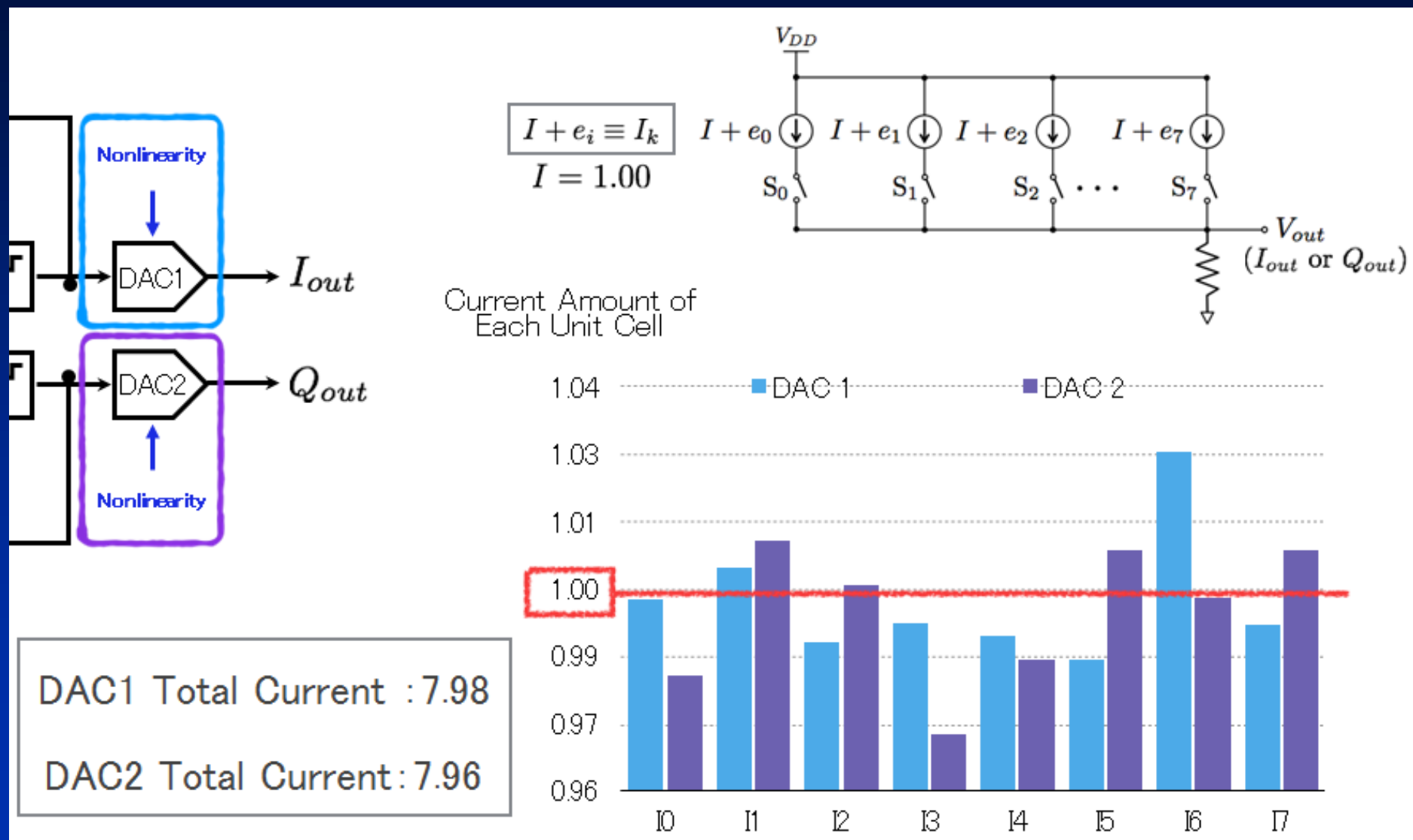


N increases → SNDR decreases

Simulation Conditions :

DAC unit cell variation

Standard deviation 1.0%



DWA = $\Delta\Sigma$

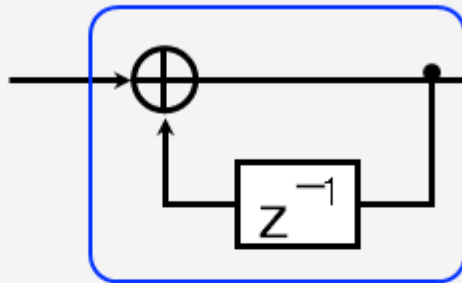
Non-Linearity

δ

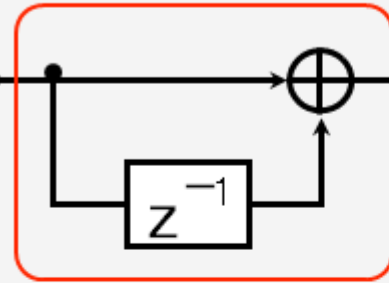
Integration

Differentiation

Input



DAC



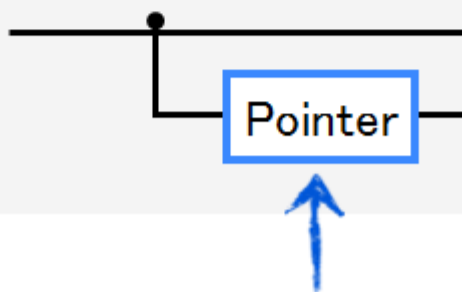
Output

δ affected by only Differentiation

Can't be realized directly

δ

Input



DAC

Output

Equivalent circuit for implementation

Memorize next cell selection start point